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Subthreshold Conduction in MOS Transistors

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Abstract

Analytical models are reviewed in this paper which accounts for drain current in subthreshold region of operation of MOS transistor. Standard modeling approaches are discussed in the form of long-channel and short channel. The comparison of the theoretical models is discussed with experimental models [1, 2]. The drain current dependence on gate bias is reviewed as subthreshold slope. Tunnel transistors having subthreshold swing less than the conventional limit are discussed.

Keywords: Subthreshold Conduction, Subthreshold Slope, Subthreshold Swing, Interband Tunnel Transistors.

NOMENCLATURE

b	Band bending parameter
C_{OX}	Gate capacitance per unit area
C_{dm}	Max Depletion capacitance per unit area
D	Electron diffusion constant
I_{DS}	Dain-Source current
I_D	Drain current
I_{DRIFT}	Drift current
$I_{DIFFUSION}$	Diffusion current
I_{SUB}	Subthreshold current
J_{SUB}	Subthreshold current density
k	Boltzmann's constant
L	Length of gate
L_B	$=\sqrt{\varepsilon_s kT/q^2 N_B}$. Extrinsic Debye Length
ϕ_t	Thermal Voltage, kT/q
ϕ_F	Fermi potential
ψ	Potential
ψ_B	Difference between Fermi level and intrinsic level
ψ_S	Surface potential
μ	Carrier mobility
μ_{eff}	Effective mobility
μ_n	Electron mobility
μ_p	Hole mobility

n	Density of free electrons
n_0	Density of electrons at thermal equilibrium
n_i	Intrinsic carrier concentration
n_n	Density of electrons in n-region
n_p	Density of electrons in p-region
N_a	Acceptor impurity concentration
N_a^-	Number of ionized charge acceptors
N_B	Bulk impurity concentration
N_d	Donor impurity concentration
N_d^+	Number of ionized charge donors
ρ	Charge density per unit volume
p	Density of free holes
p_0	Density of free holes at thermal equilibrium
p_n	Density of holes in n-region
p_p	Density of holes in p-region
γ	Body factor
E	Electric field intensity
ϵ_{Si}	Permittivity in Silicon
ϵ_{OX}	Permittivity in Oxide
q	Electronic charge (1.6×10^{-19} C)
Q	Charge
Q_d	Depletion charge density
Q_i	Inversion charge density
t_{OX}	Gate oxide thickness
S	Subthreshold slope
T	Temperature in deg. Kelvin
U_{DS}	Drain-to-source voltage normalized by kT/q
V_{bi}	Built-in potential
V_{FB}	Flatband voltage
V_{BS}	Substrate-to-source voltage
V_G	Gate voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
V_T	Threshold voltage
W	Width of gate

I. INTRODUCTION

MOS transistor technology has advanced to nanometer effective channel lengths. The physics of these advanced transistors is still been studied extensively. In simple MOSFET models, the device conducts no current until an inversion layer is formed. However, mobile carriers do not abruptly disappear the moment the gate voltage drops below V_T. It is well-known that when the gate-to-source voltage of a MOS transistor is reduced below the threshold voltage defined by the usual strong inversion characteristics, the channel current decreases approximately exponentially. This subthreshold region of

characteristics, inside which the device operates with a weakly inverted channel, has been studied by many authors.

Barron [5] has developed a pertinent theory and has obtained a solution in closed form by introducing some approximations. Troutman and Chakravarti [1] have derived a model valid for any substrate bias and extendable to short channel lengths; they have shown that channel current, in weak inversion flows by diffusion. In subsequent papers, Troutman has analyzed in more detail the effect of substrate bias [2] and the slope of the exponential characteristics [4]. Van Overstraeten *et al.* have demonstrated that this diffusion current is a function of the inversion charge at the source and drain [6].

The reason for a growing importance of subthreshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits and to keep electric fields at a lower level inside small devices, to maintain device reliability. The amount of subthreshold conduction is set by the threshold voltage, which amounts between ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction implies less gate voltage swing below threshold to turn the device off, and as subthreshold conduction varies exponentially with gate voltage, it becomes more and more significant as MOSFETs shrink in size.

The purpose of this paper is to discuss the weak inversion (or subthreshold conduction) operation of MOS transistors. A general model, based on previously mentioned work is derived in III and compared with experimental outcomes in IV using a model based approach. Subthreshold current dependence on drain voltage and temperature effects are discussed in V and VI. A theoretical subthreshold slope model is presented in VII following current trend in low-subthreshold swing tunnel transistors in VIII.

II. SUBTHRESHOLD REGION

The MOS transistor has three regions of operation in which current flows from source to drain; they are the weak inversion or subthreshold region, the moderate inversion and the strong inversion region. The subthreshold region occurs when the gate to source voltage or gate voltage V_{GS} is less than the threshold voltage V_T and the strong inversion region occurs when the gate voltage is significantly greater than the threshold voltage. The mechanism of subthreshold current flow is due to the diffusion of minority carriers when the gate voltage is several ϕ_t's less than V_T. The subthreshold current is diffusion current and the strong inversion current is drift current [6].

The intermediate region where the strong inversion and subthreshold regions meet is known as the moderate inversion region. Fig. 1 shows plot of drain current versus gate voltage for aforesaid three regions of operation. The diffusion current depends exponentially on the gate voltage, hence plotted on logarithmic scale.

Defining in terms of surface potential, ψ_S, the inversion region corresponding to a surface potential between ϕ_F and $2\phi_F$ is called weak inversion, and the region in which the surface potential is larger than $2\phi_F$ is called strong inversion. Arbitrarily, the surface potential is $2\phi_F$ at the onset of strong inversion, at which the electron concentration at the surface in the channel is equal to N_a. However, in practice surface inversion occurs well before this point and there are mobile carriers in the channel region capable of conducting current. Hence, there is a necessity to define an intermediate region between weak inversion and strong inversion. This region is moderate inversion and the surface potential for this region is within few ϕ_t's of $2\phi_F$.

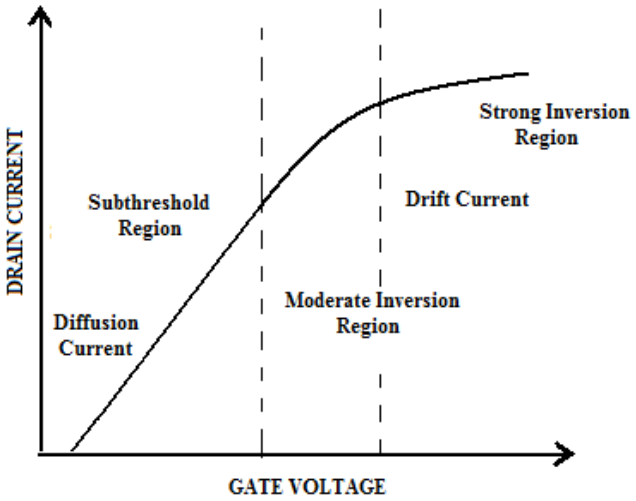

Fig. 1 The three regions of transistor operation shown on a plot of drain current versus gate voltage. The threshold voltage occurs in the transition region.

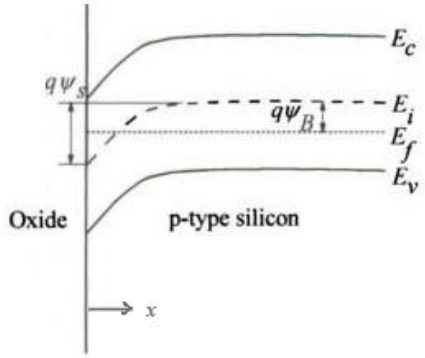

Fig. 2 Energy-band diagram near the silicon surface of a p-type MOS device.

III. SUBTHRESHOLD CURRENT EXPRESSION

We will proceed with general analysis to obtain a current expression. The subthreshold current expression involves relation among the surface potential, charge and electric field. The relation can be obtained by solving Poisson's equation in the surface region of the silicon. A more detailed energy-band diagram at the surface of a p-type silicon is shown in Fig. 2. The potential $\psi(x) = \psi_i(x) - \psi_i(x = \infty)$ is defined as the amount of band bending at position x, where $x = 0$ is at the silicon surface and $\psi_i(x = \infty)$ is intrinsic potential in the bulk silicon. $\psi(x)$ is positive when the bands bend downward. The boundary condition are $\psi = 0$ in the bulk silicon and $\psi = \psi(0) = \psi_s$ at the surface. The surface potential ψ_s depends on the applied gate voltage.

$$\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon} \qquad (1)$$

$$\frac{d\psi}{dx} = -E(x) \qquad (2)$$

Combining (1) & (2) we get Poisson's equation;

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon} \qquad (3)$$

Considering ρ as charge density in a semiconductor, for a general case there may be four sources accounting for its significance;

1)holes, which contribute a charge density of $(+q)p$;

2)free electrons, which contribute a charge density of $(-q)n$;

3)ionized donor atoms, which contribute $(+q)N_d$; and

4)ionized acceptor atoms, which contribute $(-q)N_a$.

The total charge density will then be;

$$\rho = q[p - n + N_d^+ - N_a^-] \qquad (4)$$

Charge density per unit volume at point x will then be substituted in (3),

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_{Si}}[p(x) - n(x) + N_d^+(x) - N_a^-(x)] \qquad (5)$$

In the bulk silicon $p=N_a$, $n=n_i^2/N_a$. Charge neutrality condition for a uniformly doped p-type silicon requires

$$N_d^+(x) - N_a^-(x) = -N_a + \frac{n_i^2}{N_a} \qquad (6)$$

In the surface region, $n(x)$ and $p(x)$ are given by equation (7) and (8) in terms of ψ as;

$$n(x) = n_i e^{q(\psi_i - \phi_f)/kT} = \frac{n_i^2}{N_a} e^{q\psi/kT} \qquad (7)$$

$$p(x) = n_i e^{q(\phi_f - \psi_i)/kT} = N_a e^{-q\psi/kT} \qquad (8)$$

It is inherent in (7) & (8) that for $\psi_B = \phi_F - \psi_i$ $(x = \infty)$; $e^{q\psi_B/kT} = N_a/n_i$. Substituting (6), (7) and (8) in (5) yields;

$$\frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_{Si}}\left[N_a(e^{-q\psi/kT} - 1) - \frac{n_i^2}{N_a}(e^{q\psi/kT} - 1)\right] \qquad (9)$$

Multiplying $(d\psi/dx)dx$ on both sides of (9) and integrating from bulk (ψ = 0, $d\psi/dx$ = 0) towards the surface,

$$\int_0^{d\psi/dx} \frac{d\psi}{dx} d\left(\frac{d\psi}{dx}\right)$$

$$= -\frac{q}{\varepsilon_{Si}}\left[N_a(e^{-q\psi/kT} - 1) - \frac{n_i^2}{N_a}(e^{q\psi/kT} - 1)\right]d\psi, \qquad (10)$$

which gives the electric field at x, $E = -(d\psi/dx)$ in terms of ψ,

$$E^2(x) = \left(\frac{d\psi}{dx}\right)^2 = \frac{2kTN_a}{\varepsilon_{Si}}\left[\begin{array}{l}\left(e^{-q\psi/kT} + \frac{q\psi}{kT} - 1\right) \\ + \frac{n_i^2}{N_a}\left(e^{q\psi/kT} - \frac{q\psi}{kT} - 1\right)\end{array}\right] \qquad (11)$$

Applying Gauss's Law which is another form of Poisson's

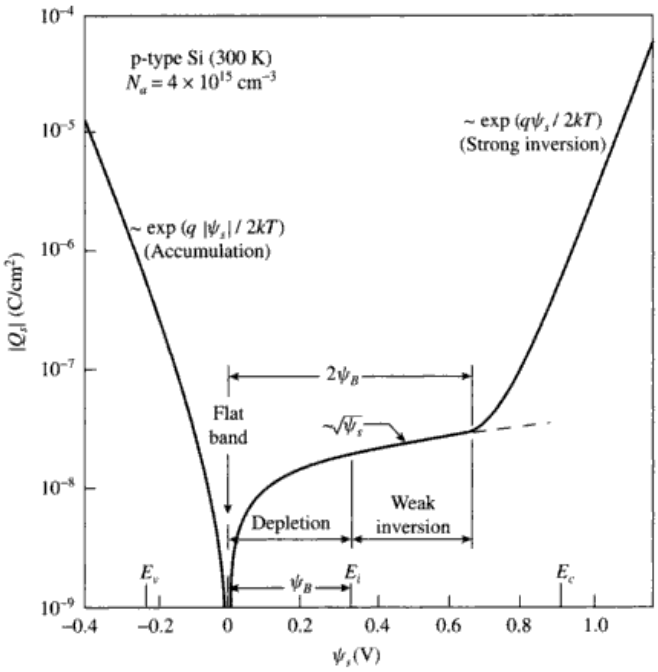

Fig. 3 Variation of total charge density (fixed plus mobile) in silicon as a function of surface potential for a p-type MOS device, [7].

equation and an integration of (3),

$$E = \frac{1}{\varepsilon_{Si}} \int \rho(x)dx = \frac{Q_S}{\varepsilon_{Si}} \qquad (12)$$

at $x = 0$, we let $\psi = \psi_s$ and $E=E_s$, the total charge per unit area in silicon is;

$$Q_S = -\varepsilon_{Si} E_S = \pm\sqrt{2\varepsilon_{Si} kTN_a}\left[\left(e^{-q\psi/kT} + \frac{q\psi}{kT} - 1\right)\right.$$

$$\left. + \frac{n_i^2}{N_a}\left(e^{q\psi/kT} - \frac{q\psi}{kT} - 1\right)\right] \qquad (13)$$

This function is plotted in Fig. 3. At the flatband condition, $\psi_s = 0$ and $Q_S = 0$. In depletion, $\psi_s > 0$ and $q\psi_s/kT > 1$, but exp ($q\psi_s/kT$) is not large enough to make the n_i^2/N_a^2 term appreciable. Therefore, the $q\psi_s/kT$ term in the square bracket dominates and the negative depletion charge density (from ionized acceptor atoms) is proportional to $\psi_s^{1/2}$. When ψ_s increases further, the $(n_i^2/N_a^2)\exp(q\psi_s/kT)$ term eventually becomes larger than the $q\psi_s/kT$ term and dominates the square bracket. This is when inversion occurs. The negative inversion charge density is proportional to exp ($q\psi_s/2kT$) as pointed in Fig. 3.

A well-known criterion for the onset of strong inversion is for the surface potential to reach a value such that $(n_i^2/N_a^2)\exp(q\psi_s/kT) = 1$. Under this condition, the electron concentration is given by (7) at the surface becomes equal to the depletion charge density N_a. After the inversion takes place, even a slight increase in the surface potential results in a large buildup of electron density at the surface. The inversion layer effectively shields the silicon from further penetration of the gate field. Since almost all of the incremental charge is taken up by electrons, there is no further increase of either the depletion charge in the depletion-layer width. As our intention in this analysis is to come up with a current

expression, we will directly focus on weak inversion analysis further.

Fig. 4 shows the schematic cross section of an n-channel MOS transistor in which the source is the n+ region on the left, and the drain is the n+ region on the right. $\psi(x, y)$ is the band bending or intrinsic potential at point (x, y) with respect to the bulk intrinsic potential. Assume that $V(y)$ is the electron quasi-Fermi potential at a point y along the channel with respect to the Fermi potential of the n+ source. Since there is no bias between the source and the substrate, the Fermi potential of the source is the same as that of the bulk. The quasi-Fermi potential stays essentially constant across the depletion region, *i.e.* $V(y)$ does not change with x in the direction perpendicular to the surface.

A key assumption in one-dimensional analysis of MOS transistor is the gradual channel approximation, which assumes that the variation of the electric field in the y-direction is much less than the corresponding variation in the x-direction [3]. The same further assumes that both the hole current and the generation and recombination current are negligible, so that the current continuity equation can be applied to the electron current in the y-direction, *i.e.*, the total drain-to-source current I_{DS} is same at any point along the channel. Thus the electron current density at any point (x, y) is;

$$J_n(x, y) = -q\mu_n n(x, y)\frac{dV(y)}{dy} \qquad (14)$$

where μ_n is the electron mobility in the channel. Total current at a point y along the channel is then obtained by multiplying (14) with the channel width W and integrating over the depth of the inversion layer. The limits for the integration are carried out from $x = 0$ to x_i,

$$I_{DS}(y) = qW\int_0^{x_i} \mu_n n(x, y)\frac{dV(y)}{dy}dx \qquad (15)$$

A sign change should be noticed as we define $I_{DS} > 0$ to be the drain-to-source current in the y-direction. Since V is a function of y only, dV/dy can be taken outside integral. Also assume that μ_n will now be replaced by $\mu_{eff.}$ What is left in the integral is $n(x, y)$. Its integration over the inversion gives the inversion charge per unit gate area, Q_i;

$$Q_i(y) = q\int_0^{x_i} n(x, y)dx \qquad (16)$$

(15) now becomes,

$$I_{DS}(y) = -\mu_{eff} W\frac{dV(y)}{dy}Q_i(y) = -\mu_{eff} W\frac{dV(y)}{dy}Q_i(V) \quad (17)$$

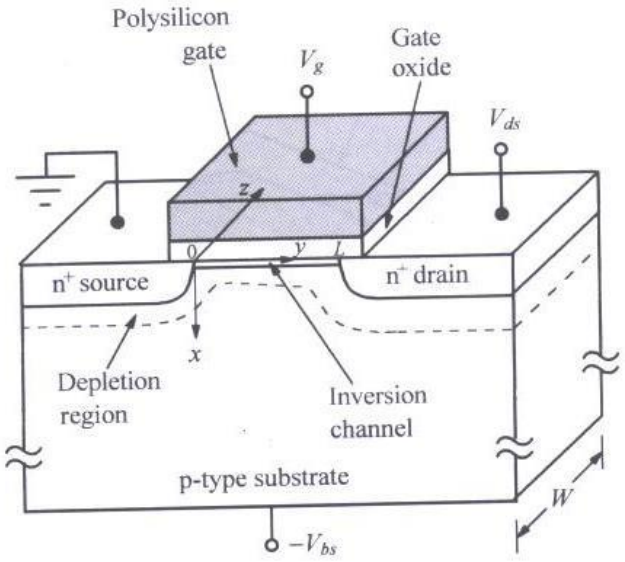

Fig. 4 A schematic MOSFET cross section showing the axes of co-ordinates and the bias voltages.

Multiplying both sides of (17) by *dy* and integrating from 0 to *L* yield,

$$\int_0^L I_{DS}\,dy = \mu_{eff} W \int_0^{V_{DS}} [-Q_i(V)]dV \qquad (18)$$

$$I_{DS} = \mu_{eff} \frac{W}{L} \int_0^{V_{DS}} [-Q_i(V)]dV \qquad (19)$$

To find an expression for subthreshold current, let's analyze (11) further. After keeping the significant terms;

$$-Q_S = \varepsilon_{Si} E_S = \sqrt{2\varepsilon_{Si} kTN_a} \sqrt{\frac{q\psi_S}{kT} + \frac{n_i^2}{N_a} e^{q(\psi_S - V)/kT}} \qquad (20)$$

where only two significant terms are kept in the square bracket. In weak inversion, the second term in the bracket arising from the inversion charge density is much less than the first term from the depletion charge density. (20) can be expanded into a power series: the zeroth-order term in the depletion charge density $-Q_d$, and the first-order term gives the inversion charge density,

$$-Q_i = \sqrt{\frac{\varepsilon_{Si} qN_a}{2\psi_S}} \left(\frac{kT}{q}\right)\left(\frac{n_i}{N_a}\right)^2 e^{q(\psi_S - V)/kT} \qquad (21)$$

The surface potential ψ_S is related to the gate voltage through,

$$V_G = V_{FB} + \psi_S - \frac{Q_S}{C_{OX}}$$
$$= V_{FB} + \psi_S + \frac{\sqrt{2\varepsilon_{Si} kTN_a}}{C_{OX}} \sqrt{\frac{q\psi_S}{kT} + \frac{n_i^2}{N_a^2} e^{q(\psi_S - V)/kT}} \qquad (22)$$

Since the inversion charge density is small, ψ_S can be considered as a function of V_G only, independent of *V*. This also means that electric field along the channel direction is small; hence the drift current is

negligible.

Substituting Q_i into (19) and carrying out integration, the expression that we obtain is the expression for the drain current in subthreshold region;

$$I_{DS} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\varepsilon_{Si} q N_a}{2\psi_s}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i}{N_a}\right)^2 e^{q\psi_s / kT} (1 - e^{-qV_{DS} / kT}) \quad (23)$$

IV. Subthreshold Conduction Model

The subthreshold behavior depends vitally on the potential distribution in the semiconductor material, and the channel length is a key parameter in determining this distribution, Troutman [2] conceptually distinguishes between two cases, *viz*. the long channel case and the short channel case. Troutman and Chakravarti [1] have considered the underlying physical mechanism of the subthreshold region and presented a simple model valid for any substrate bias and further which may be readily extendable to short-channel lengths. They have analyzed the general one-dimensional model of Pao and Sah as a starting point reference [3].

In the long channel case, the drain voltage influence is minimal on the electric field pattern between source and drain. In this case the channel length L is very long compared to the depletion width around the drain diffusion, and the high proportion of electric field lines terminating on the ionic charge near the surface originate on the gate. As the gate voltage increases above flatband, the amount of band bending at the surface increases independent of distance from the source and it is calculated by solving a one-dimensional Poisson's equation in a direction normal to the surface. Because an equilibrium minority carrier concentration is maintained at the source end, the gate voltage in terms of the band bending is incorporated into the boundary condition at the source end. The drain voltage is incorporated into a boundary condition at the drain end.

The current that results from an injection of minority carriers from the source, is caused by the surface band bending and collection of these minority carriers by the reverse-biased drain. In the subthreshold region, the injected carrier concentration is small compared to the bulk doping concentration, so the current flow is by diffusion. Troutman [2] has demonstrated for the long channel case that the minority carrier concentration decreases linearly from a value n_0, at the source end to essentially zero at the drain end for drain-to-source voltage much in excess of $3kT/q$. In addition, the subthreshold current can be described as a constant current density flowing to a depth from the surface equal to the extrinsic Debye length $L_B = \sqrt{\varepsilon_s kT / q^2 N_B}$., i.e.,

$$I_{SUB} = (WL_B)J_{SUB} \quad (24)$$

The subthreshold current density in the long channel case is given by [1],

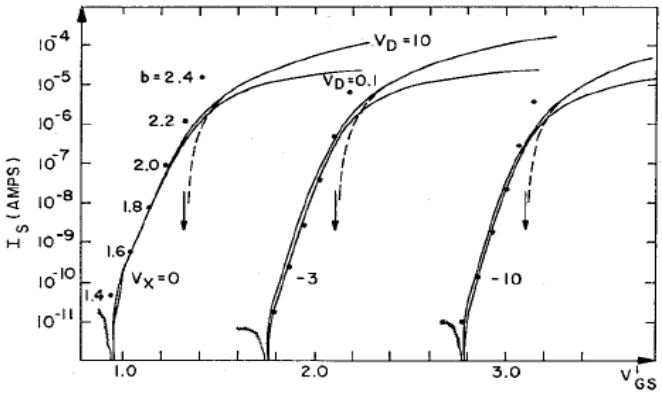

Fig. 5 Experimental subthreshold characteristics for a long-channel device (L = 15.5 um), [2].

$$J_{SUB} = = \frac{qDn_0}{L}[1 - \exp(-U_{DS})]. \qquad (25)$$

where, D is electron diffusion constant and U_{DS} is drain-to-source voltage normalized by kT/q.

In the short-channel case, the effect of drain voltage on the field pattern between source and drain is not negligible, and the device is said to exhibit "short channel" effects. Now the surface band bending is a function of position along the surface, and, the one-dimensional Poisson equation no longer provides a correct relation between the amount of band bending and the gate voltage. However, the subthreshold current is controlled by a potential barrier, and the peak of the barrier occurs where the band bending at the surface is a minimum. Since the longitudinal electric field is zero at this point, the amount of band bending for zero applied drain voltage, can still be calculated from the one-dimensional Poisson equation.

Referring Fig. 5 the onset of subthreshold current is quite clear since the channel current flows in a direction opposite to any generation current collected at the source. As the gate voltage is increased above the weak inversion point, the channel current increases to a level comparable to the generation current. The source current then sharply reverses direction and exhibits a steep rise for any further increase in gate voltage. The generation level is observed to increase with increasing substrate bias.

The experimental curves are plotted for 0.1 V and 10 V for the drain voltage values, and is it observed that for the long channel case the curves show virtually no dependence on drain voltage in the subthreshold region. Over the entire range of applied biases, the curves show less than a 10-mV shift in the subthreshold region. Once the gate voltage exceeds threshold, the device enters the linear region for V_D = 0.1 and saturation for V_D = 10. The dots indicate points calculated from the one-dimensional model at the specified levels of band bending. It is observed that the current level for a given band bending depends on substrate bias.

For comparison, the dashed curves show the saturation curve for each substrate bias extrapolated to low current values. It is observed that these extrapolated thresholds do not occur for a band-bending parameter, b of 2.0 but more nearly 2.2, and that they occur where the current characteristics are neither exponential nor quadratic. Since the reverse-biased drain is extracting minority carriers, a strongly inverted layer has just begun to form at the source when b = 2.0[1]. An additional increase in gate voltage is required to have the inversion spread across the surface to the vicinity of the drain, and a fundamental

[1] b = 1 at weak inversion and b = 2 at strong inversion [2]

assumption in the derivation of the saturation characteristics is that the current behavior is ohmic except in the immediate vicinity of the drain.

The same experimental results for the short channel case are given in Fig. 6. The shift is quite obvious in the curves to lower V_{GS}' caused by the increased drain voltage. Moreover, operation at the higher substrate voltages, even for V_D = 0.1, also causes a shift in the curves to lower gate voltages. As pointed out in the discussion of experimental low current characteristics [2], the substrate bias has a strong influence on the injection characteristics at the source. Although the source-to-substrate bias impedes subsurface injection (consequently increasing the punchthrough voltage, V_{PT}), it causes the surf ace injection for a particular device to depend more strongly on drain voltage.

The shifts due to both increased drain and increased substrate voltage are seen to agree well with the data. It is interesting to note that in spite of the shift, the shape of the curves remain essentially unchanged. Thus, even in the short channel case, the subthreshold current increases exponentially with gate voltage, and the exponential slope can be calculated as for the long channel case. However, the electron concentration at the source has been increased by the effect of drain voltage on the potential distribution at the source.

V. Dependence of Subthreshold Current upon Drain Voltage

Taylor [9] discusses the dependence of subthreshold current upon the drain voltage. For the MOS device in the subthreshold region of operation there are different modes of conduction, each of which determine the channel current for a particular range of gate and drain voltage (V_{GS} and V_{DS}). The variation of current as a function of drain voltage is of particular interest as the length of the channel is reduced. For very small drain voltages the channel diffusion current is of the order of the thermal equilibrium drift current flowing from the drain into the channel. Hence the current varies exponentially with the drain voltage in the same fashion as in a reverse-biased junction at low drain voltages. As the drain voltage is increased, the depletion region associated with the drain (Region III in Fig. 7(b)) extends towards the source and the current exhibits a significant dependence on drain voltage. If the channel length is small, enough punchthrough of the source and drain depletion regions (region I and region III) occurs at a voltage $V_{DS} = V_{PT}$ before avalanche breakdown has occurred at the drain.

VI. Effect of Temperature on Subthreshold Current

Troutman [2] presents another important design consideration is to insure that the IGFET operates in the

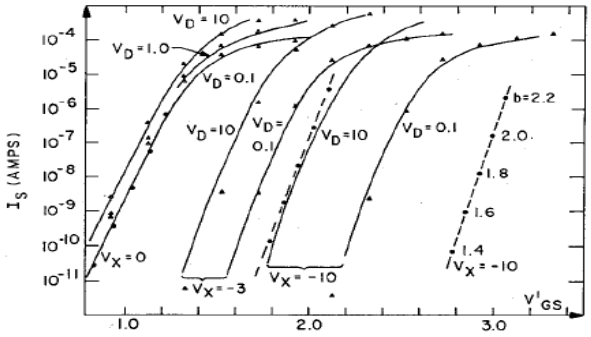

Fig. 6 Experimental subthreshold characteristics for a short-channel device (L = 2.1 um). Points shown are calculated from 0ne-dimensional model and the triangles from two-dimensional model [2].

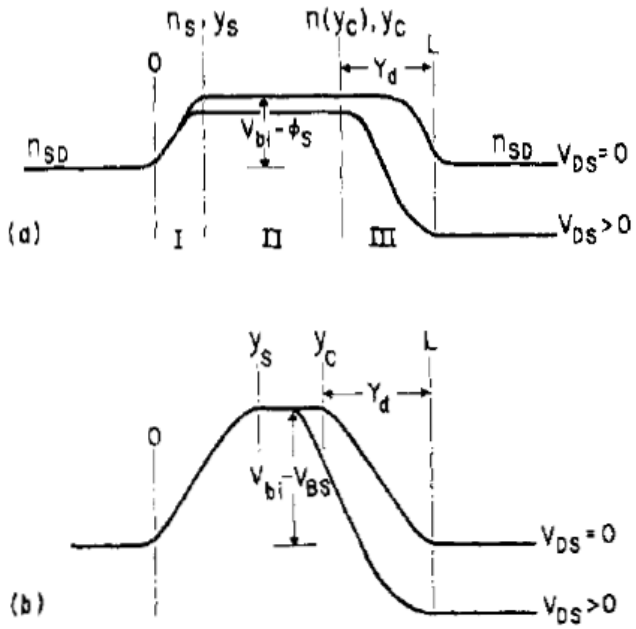

Fig. 7 MOS device and associated channel potential in the subthreshold region (a) at the surface and (b) below the surface. [9]

enhancement mode over the entire temperature range of operation. The temperature dependence of the subthreshold current at zero substrate bias is illustrated in Fig, 8. These curves have been calculated using the simple one-dimensional model for the same t_{ox} and N_B considered previously. Not only does the threshold voltage decrease with increasing temperature, but the exponential slope of the subthreshold curve also decreases, resulting in an even greater shift of the weak inversion potential, The exponential slope is shown to be inversely proportional to temperature. The dashed curves are the loci for a constant band bending parameter *b*. Note that the current at the threshold point (b = 2) increases with increasing temperature.

Also its is observed from Fig. 8 that operating an IGFET below room temperature causes the threshold voltage to increase and the slope of the subthreshold current characteristics to increase. Thus, the turn-on characteristics are sharper, and it is possible to design at a lower threshold voltage and still operate strictly in the enhancement mode.

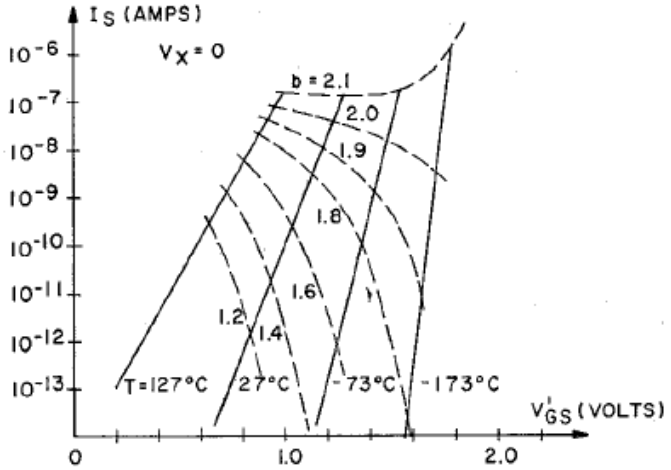

Fig. 8 Dependence of subthreshold current on temperature for t_{ox} = 570 Å, N_B = 5.6 x 10^{15} cm^{-3} and Vx = 0, [2]

This behavior can be a definite advantage if it is desired to reduce the power supply voltages as much as possible.

VII. SUBTHRESHOLD SLOPE

The subthreshold current is independent of the drain voltage once V_{DS} is larger than a few ϕ_t, as would be expected for diffusion-dominated current transport. It is evident that I_D depends exponentially on gate bias, V_G, The plot in Fig. 9 shows log I_D as a function of gate bias, V_G which is a linear region in subthreshold regime. The reciprocal of the slope of this line is known as subthreshold slope, S which has typical values of ~70mV/decade at room temperature.

By definition subthreshold slope is given by [8]:

$$S = \left(\frac{\log 10}{d(\log I_D) / dV_G} \right) = 2.3 \frac{kT}{q} \left[1 + \frac{C_{dm}}{C_{OX}} \right] \qquad (26)$$

The capacitor ratio tells us what fraction of the applied gate bias, V_G appears at the Si-SiO_2 interface as the surface potential. Apparently it is the surface potential that is responsible for modulating the barrier between source and drain, and therefore the drain current. Hence, S is a measure of the efficiency of the gate potential in modulating I_D. Observing (26), S is improved by reducing the gate oxide thickness, which is reasonable because if the gate electrode is closer to the channel, the gate control is obviously better. For very small gate voltage, the subthreshold current is reduced to leakage current of the source/drain junctions.

Troutman [4] shows a subthreshold slope expression as;

$$S = 2.3 \frac{kT}{q} \frac{1}{P} \left[1 + \frac{G t_{OX} N_B^{1/2}}{\left[V_{SX} + (b \ln N_B / n_i - 1)(kT/q) \right]^{1/2}} \right] \qquad (27)$$

VIII. LOW-SUBTHRESHOLD-SWING TUNNEL TRANSISTORS

In conventional MOSFETs the subthreshold swing is limited to (kT/q) ln10 or 60mV/decade at room temperature. The subthreshold swing increases with scaling, [10]. A common

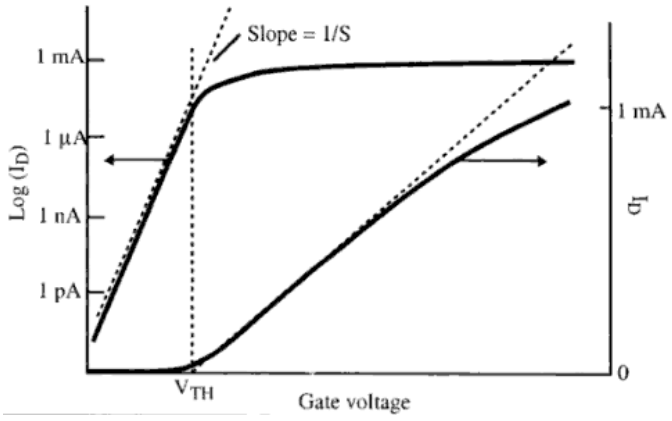

Fig. 9 Drain current in both linear and logarithmic scales (V_{DS} is small)

limitation observed in conventional MOSFETs is the subthreshold swing increases as the gate length is decreased. It is been reported in [11] that certain interband tunnel transistors can have subthreshold

swings below 60mV/decade and that subthreshold swing is minimized by engineering the transistor geometry to enhance the gate control of the tunnel-junction bias-voltage and internal electric field.

The first tunneling device which has an SS less than 60 mV/decade was implemented by Appenzeller *et al.* [12] based on carbon nanotube technology. In the carbon nanotube field-effect transistor of Appenzeller *et al.* [12], a subthreshold swing of 40 mV/decade was measured in a doublegated transistor in which interband tunnel current flows through an n-p-n channel modulated by a top gate. In simulations, Bhuwalka *et al.* [13] have shown in a vertical gated p-i-n Si/SiGe interband tunneling transistor that subthreshold swings of 44 mV/decade can be achieved. In a lateral embodiment of the p-i-n Si interband tunnel transistor, Wang *et al.* [14] have shown by simulations that subthreshold swings of 15 mV/decade and even smaller are achievable and conclude that the subthreshold swing is not limited by *kT/q*. Zhang *et al.* [11] provided a theoretical analysis for the low SS in tunnel transistors and proposed a new transistor configuration demonstrating that the SS value can be reduced below 60 mV/decade.

IX. SUMMARY

This paper discusses the analytical modeling weak inversion (or subthreshold conduction) operation of MOS transistors referring existing literature. A general model, based on previously mentioned work is reviewed and compared with experimental outcomes. A figure of merit, subthreshold slope is discussed and current trends in device technology are reviewed pertaining to the minimum limit of subthreshold slope. It is observed that current devices offer a significant amount of reduction in subthreshold slope which is a good indication for future device technology.

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