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Design of CMOS Operational Amplifier with High Voltage Gain and Low Power Consumption

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Abstract

Operational amplifiers (op-amps) are vital components in modern electronics, serving as versatile building blocks in analog circuits for applications ranging from signal amplification to filtering and data conversion. This paper explores the design principles and methodologies for creating efficient operational amplifiers that meet diverse performance requirements, including high gain, wide bandwidth, low noise, low power consumption, and adaptability to specific use cases.

The design process typically involves selecting appropriate architectures such as single-stage, two-stage, or multi-stage configurations, each tailored to achieve specific trade-offs in gain, stability, and power efficiency. Key considerations include the choice of transistor technology (e.g., CMOS, bipolar), biasing techniques, and topology optimizations like cascoding and feedback mechanisms to enhance performance metrics. Modern advancements leverage computational optimization techniques, such as Quantum-Behaved Particle Swarm Optimization (QPSO), to streamline the selection of design parameters, improving precision and reducing convergence time compared to traditional methods [2].

This paper also discusses specialized design approaches for low-power and low-noise op-amps, crucial in portable and precision instrumentation. Techniques such as rail-to-rail input stages, folded cascodes, and class-AB biasing are analyzed for their ability to maximize output voltage swing and efficiency. Furthermore, flexible architectures [7], like reconfigurable multi-stage designs, provide adaptability for applications requiring variable performance profiles.

Design validation is performed through simulation and experimental testing using industry-standard tools such as Cadence Virtuoso and OrCAD, ensuring compliance with specifications for key metrics such as gain, bandwidth, slew rate, and power dissipation. The results demonstrate that carefully tailored design strategies, supported by simulation-driven optimization, enable the creation of robust and efficient operational amplifiers suited for a wide array of modern electronic applications. These insights offer a framework for advancing op-amp designs to meet evolving technological demands [1].

Keywords: Operational Amplifier Design, Low Power Consumption, High Gain and Bandwidth, CMOS Technology, Optimization Techniques

1. Introduction

Operational amplifiers (op-amps) are fundamental components in modern analog electronics, playing a crucial role in various applications such as signal processing, data conversion, filtering, and control systems. These versatile devices amplify electrical signals and are indispensable in industries ranging from consumer electronics to aerospace, biomedical instrumentation, and communications. The design

of operational amplifiers requires a deep understanding of both theoretical principles and practical constraints to achieve optimal performance.

An operational amplifier is typically designed to meet specific performance metrics, including high open-loop gain, wide bandwidth, low noise, low offset, and minimal distortion. Other critical considerations include power efficiency, which is essential for battery-operated systems, and flexibility to adapt to diverse operational requirements [10]. The design process involves careful selection of topology, such as single-stage, two-stage, or multi-stage configurations, to balance trade-offs between gain, stability, and bandwidth. For instance, single-stage amplifiers offer simplicity and speed, while multi-stage amplifiers can achieve high gain and better control over frequency response. Modern advancements in operational amplifier design have introduced techniques to enhance performance under stringent constraints. Low-power designs, for instance, incorporate rail-to-rail input stages and class-AB output stages to maximize voltage swings while minimizing power consumption [3]. Additionally, high-precision applications demand designs with ultra-low noise and distortion, which are achieved through techniques such as folded cascades and precision biasing.

With the evolution of semiconductor technology, CMOS-based designs have become the dominant approach, offering advantages in scalability, integration, and power efficiency. Computational methods, such as genetic algorithms and Quantum-Behaved Particle Swarm Optimization (QPSO), are increasingly employed to optimize design parameters, accelerating the development process and ensuring high precision [5].

Validation of operational amplifier designs typically involves a combination of simulation and experimental testing using advanced tools like Cadence Virtuoso and SPICE-based simulators [4]. These tools allow engineers to fine-tune performance metrics and verify compliance with design specifications.

In summary, the design of operational amplifiers is a multidisciplinary endeavor that combines electronics theory, optimization techniques, and practical considerations. It continues to evolve, driven by the demand for higher performance, energy efficiency, and integration into complex systems [6]. This paper explores the key principles, methodologies, and advancements that underpin the development of modern operational amplifiers.

2. Design Specifications

A single stage differential input and single-ended output amplifier with a power supply of 1.8volts. Amplifier has an internal current source generated with self-bias circuit with the startup circuit. CMOS 0.35mm technology is used in the design of an amplifier.

- Differential voltage gain: Avd > 85 dB.
- Output voltage swing range: OVSR = Vo(max) – Vo(min) > 1.4 V.
- Average slew rate: SR > 10 V/us
- Common mode rejection ratio: CMRR > 80 dB.
- Unity-gain bandwidth: GBW > 8 MHz.
- Phase margin: f(GBW) > 60 deg.
- Power dissipation (VDD): Pdiss ≤ 0.35 mW (1.8V)
- Capacitive load: 3 pF

These approximations are considered for the hand calculations, and the values are fine-tuned after the recursive simulations.

For NMOS:

- Vth 0.55 V
- μn * Cox 180 μA/V2

For PMOS:

- Vth - 0.7 V
- μp * Cox 60 μA/V2

3. Design Methodology

- From the Project specifications, derived the minimum current at the output to meet the slew rate specifications with the given capacitive load.
- Once the minimum current (with one branch is off) required is derived, derive the currents for the branches of the folded cascade. In our design we have taken equal currents in both the cascaded structure and the input transistor branches.
- From the output voltage swing specifications, we have assigned the over drive voltages for the cascade structures to meet 1.4 Volts output swing. We have calculated for 0.1v overdrive for each transistor in the cascade structure results 0.4 volts drop, and 1.4 volts output swing.
- Once the overdrive voltages of all the transistors are derived, we have computed the (W/L) ratios of the individual transistors with the approximate values of threshold voltages & μ * Cox.
- From the overdrive voltages, and currents in the particular cascade structures, derived the biasing voltages required for the cascade transistors.
- From the above calculations, we have derived the required biasing voltages & currents, now we have designed the self-bias circuit with the derived current value and startup circuit for the protection of the self-bias. Also designed the bias voltages references from the generated current.
- Input common mode voltage is calculated by summing the input MOS source voltage & threshold voltage & overdrive required to pass the expected current.
- We have considered the length of the MOS transistors as 2um for the current mirrors to minimize the effect of channel length modulation. Also, we have considered the length of cascade MOS transistors (4 trans in the middle of the cascade) to have large resistance to improve the gain of the amplifier, and the rest of the amplifier's length is considered as 1um.
- We made sure, current in the cascode branches to be same as derived from the slew rate specifications during the process of improving the gain, so the slew rate specification is not disturbed in achieving the voltage gain.
- Voltage gain is improved by increasing the (W/L) ratios of the amplifying transistors & cascode transistors, with the following changes, current is adjusted by modifying the current mirrors ratios.

Amplifying transistors: M16, M17

Cascode transistors: M2, M3, M4, M5

4. Design Schematic

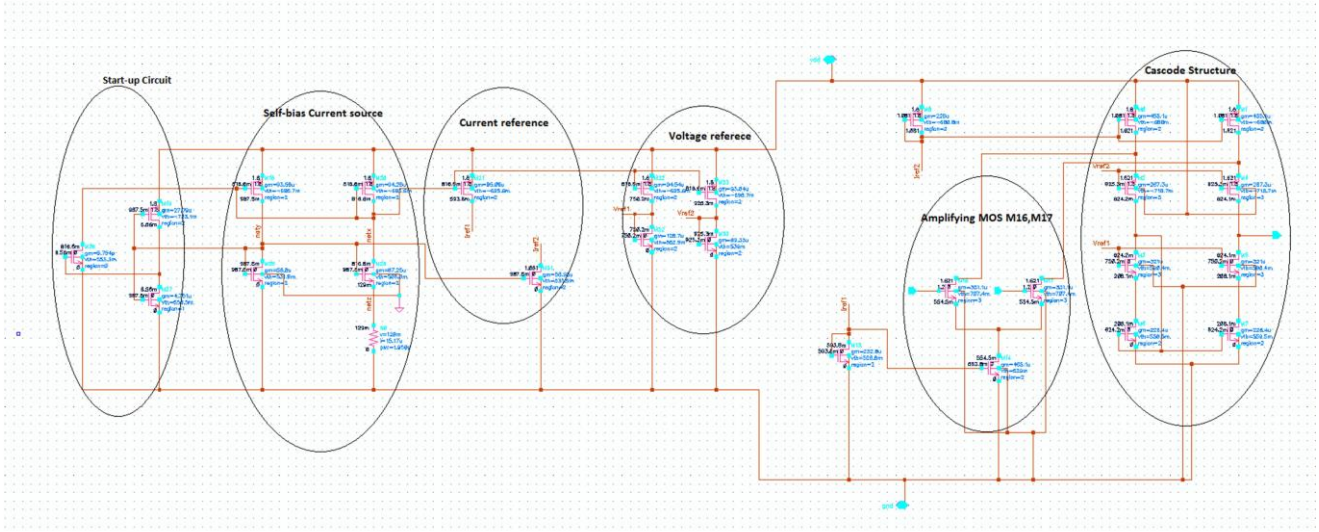

Figure 1: Schematic of an Operational Amplifier

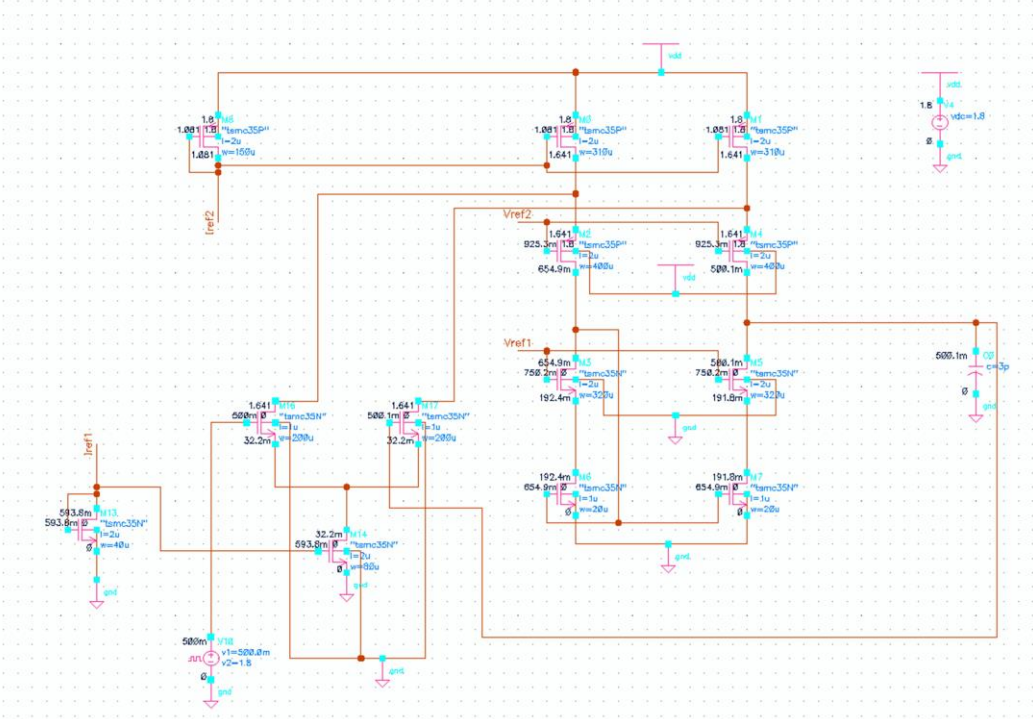

Figure 2: Schematic of the Folded Cascode amplifier

Transistor Name	Width (µm)	Length (µm)	Transistor Name	Width (µm)	Length (µm)	Transistor Name	Width (µm)	Length (µm)
M0	310	2	M7	20	1	M19	5	1
M1	310	2	M8	150	2	M20	12.5	2
M2	400	2	M13	40	2	M21	12.5	2
M3	320	2	M14	80	2	M22	12.5	2
M4	400	2	M16	200	1	M23	12.5	2
M5	320	2	M17	200	1	M26	5	1
M6	20	1	M18	12.5	2	M27	5	1
M28	2.5858	1	M31	1.1092	1	M33	1.45	1
M29	1.1092	1	M32	4.42	1			

5. Frequency Analysis

Bias current source: 15uA
Non-inversing input: DC-1.2V I
Inverting input: DC-1.2V, AC-1V.

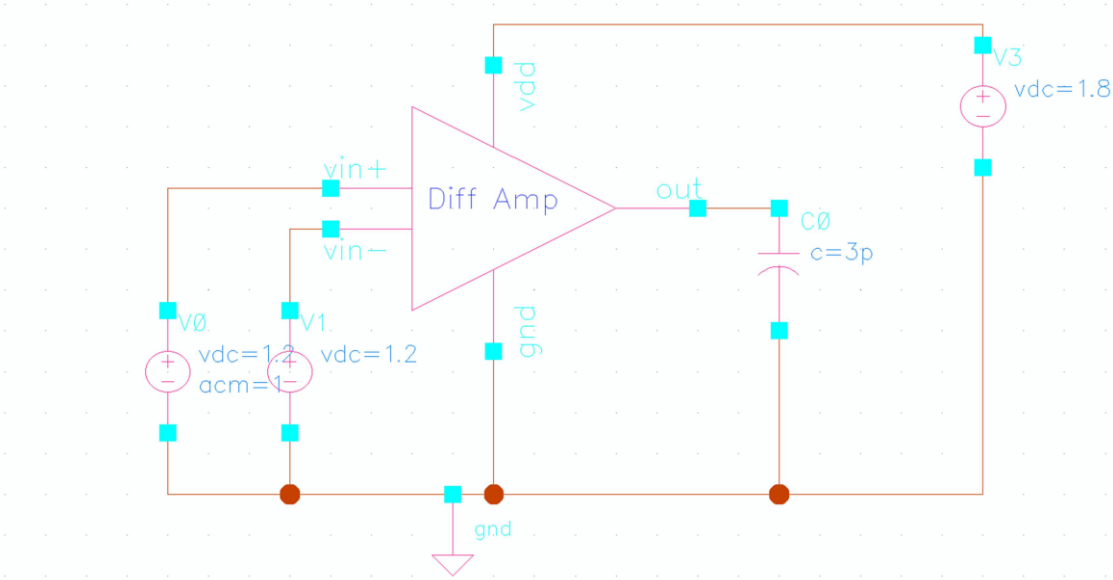

Figure 3: Test setup for the AC analysis

We simulated the AC analysis by varying the frequency from 0 to 20 MHz and plotted the AC-gain-and-phase graph as shown in Fig. We have simulated the following results:

- Differential gain: 79.05dB 85db (Design spec.)
- Unity gain bandwidth: 15.43 MHz 8 MHz (Design spec.)
- Phase margin: 61.4 deg. 60 deg.(Design spec)

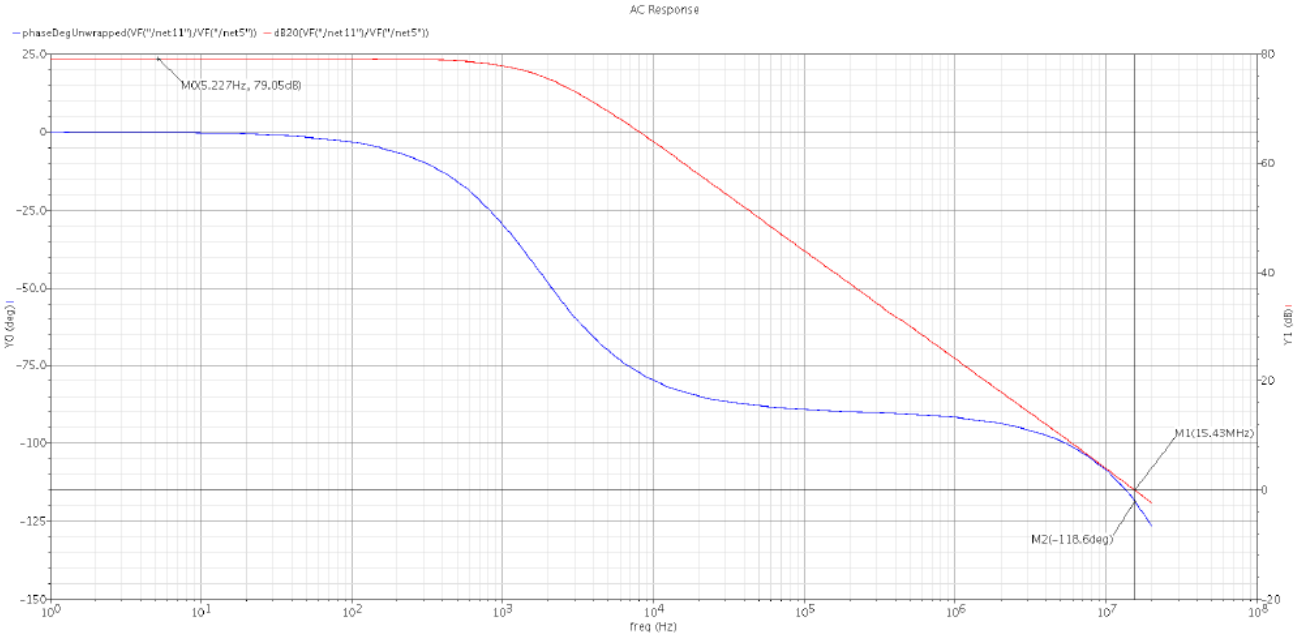

Figure 4: Operational amplifiers AC analysis

From the AC analysis, the power required for the operational amplifier to operate id derived by computing the current drawn from the 1.8V power supply and multiplying the current drawn & voltage.

- Power = current_drawn * 1.8v
- Power = 153.9u * 1.8v
- Power = 0.277 mW

Common mode voltage gain is simulated by shorting the inverting & non-inverting terminals of the operational amplifier and simulating the AC analysis by varying the frequency from 0 to 20 MHz, the result is plotted with AC-gain and-phase graph. Inverting & non-inverting terminals are set to DC-1.5v & AC-1V

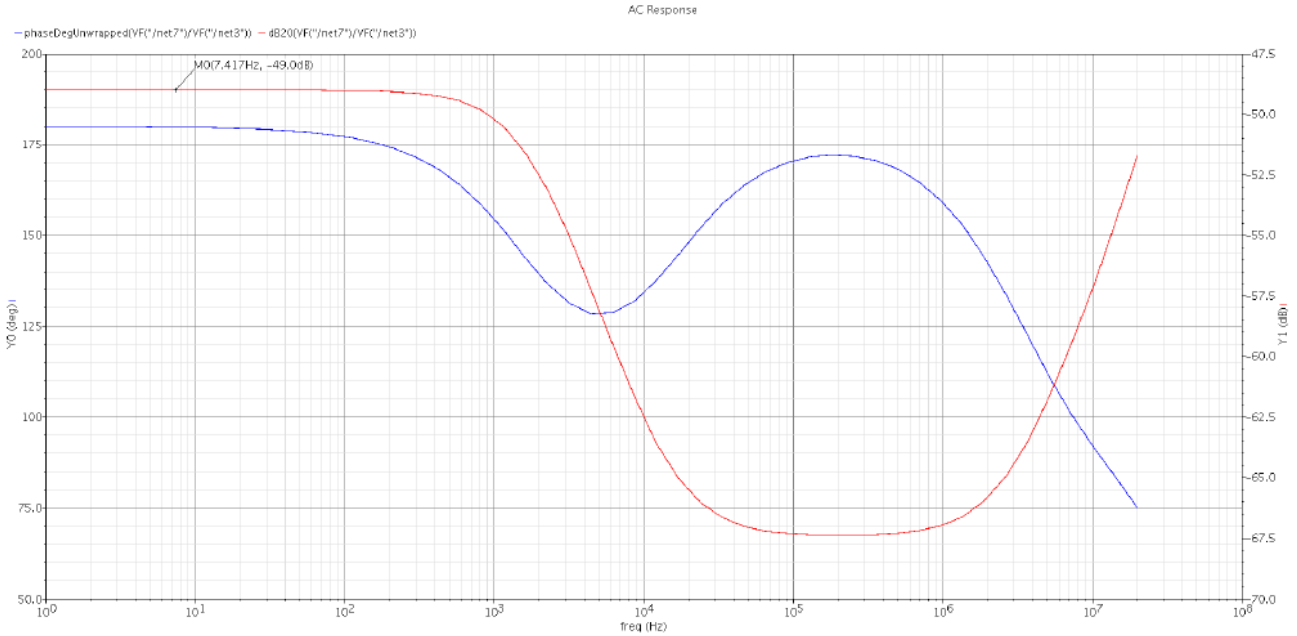

Figure 5: Operational amplifier Common mode gain

Common mode rejection ratio is difference between the differential voltage gain (in dB) & common mode gain.

- CMRR = Avd (dB) – Acm (dB)
- CMRR = 79.05dB – (-49dB)
- CMRR = 128.05dB

6. Output Voltage Swing

To check the OVSR, we have connected the operational amplifier in negative feedback. The value of the feedback resistor is 50K (Rf) ohms & the value of the input (inverting terminal) is 1K ohms (Rg).

Inverting terminal relates to output feedback with a resistor of 50K ohms, and DC voltage at 1.3v. non-inverting terminal relates to DC voltage at 1.3V, and additional DC source by specifying the design variable, and simulating the DC analysis by varying the design variable (voltage at non-inverting terminal) from -200mv to 200mv. Since the operational amplifier is connected in feedback mode, gain is derived from the formula below

$$V_{\text{out}} = V_{\text{in}} + i \times R_f = V_{\text{in}} + \left(\frac{V_{\text{in}}}{R_g} \times R_f\right) = V_{\text{in}} + \frac{V_{\text{in}} \times R_f}{R_g} = V_{\text{in}}\left(1 + \frac{R_f}{R_g}\right)$$

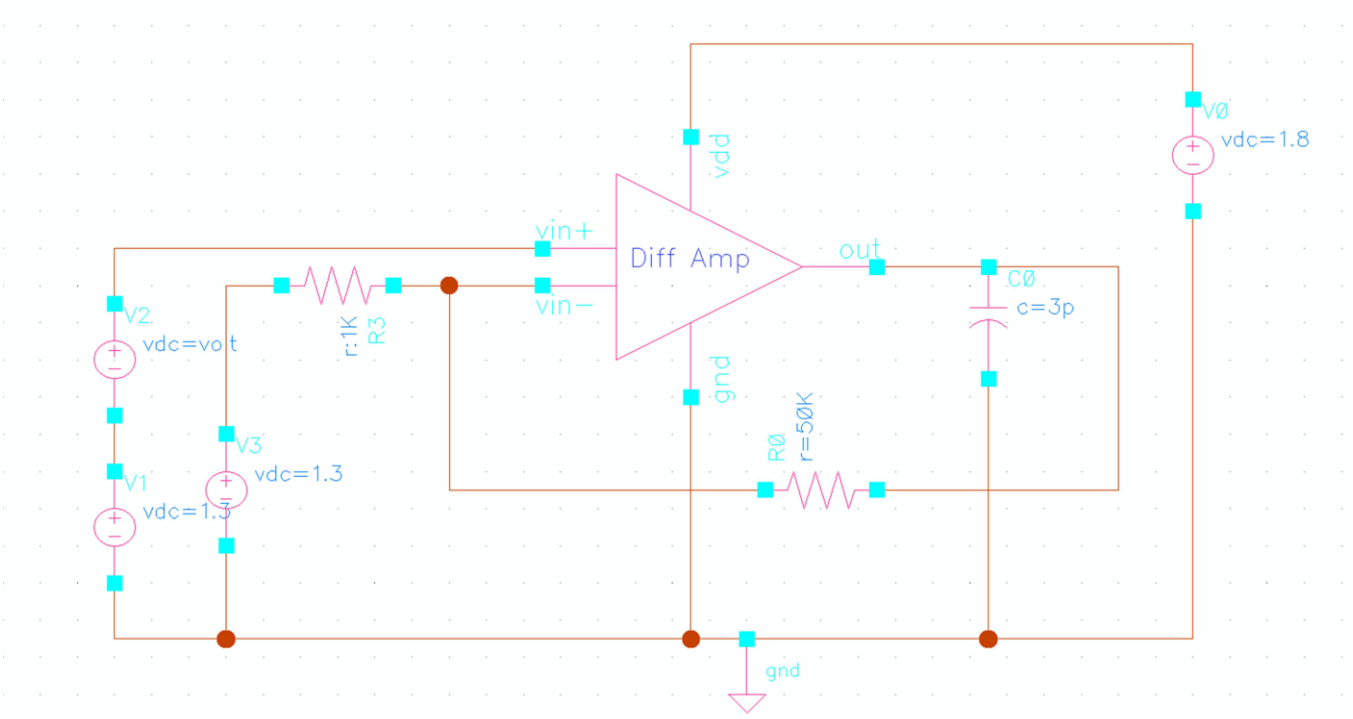

Figure 6: Test setup to calculate output voltage swing

Simulation result from the graph: Output voltage swing is : Voh – Vol
Output Voltage swing = 1.644v – 0.233v = 1.411

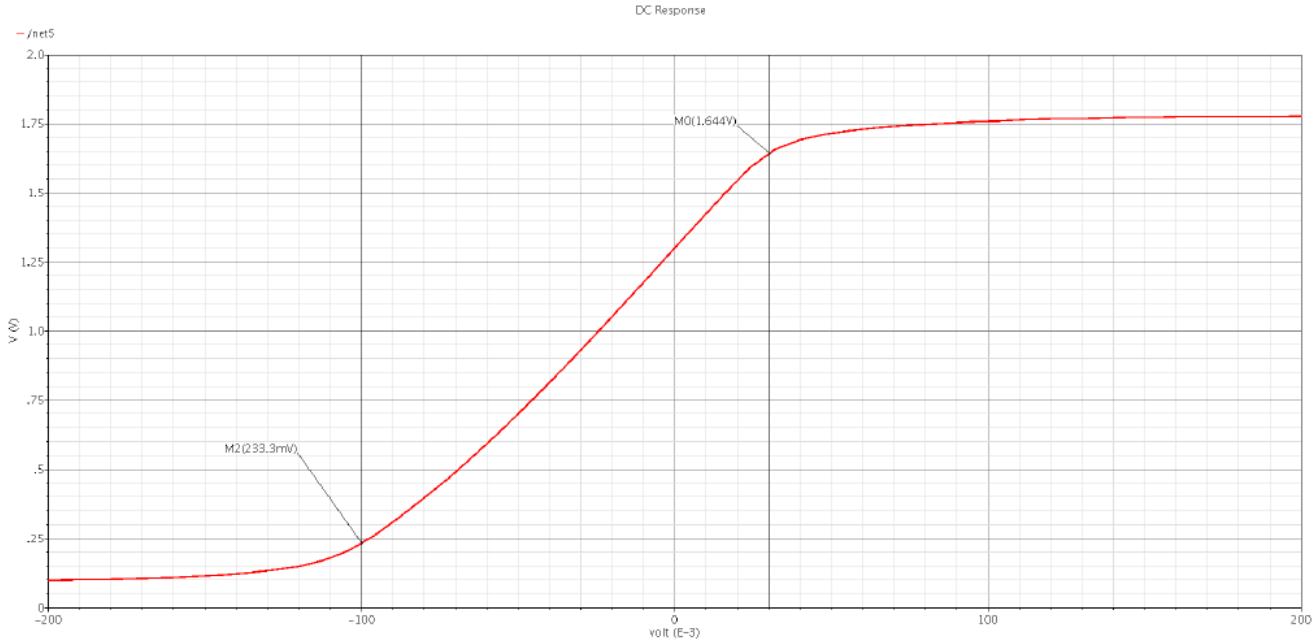

Figure 7: Operational amplifier Output voltage swing

7. Slew Rate

To compute the slew rate we connected the operational amplifier in unity gain feedback mode by shorting the output to the inverting terminal. Non-inverting terminal is connected to pulse voltage supply with the low voltage is equal to 0.5v and the high voltage is equal to 1.8v, and the period is set to 2us

with equal on time & off time. We simulated the transient analysis and measured the slew rate with the 20% - 80% of the rising slope, and 80% - 20% of the falling slope.

- Positive slew rate = 8.5V/us
- Negative slew rate = 8.32V/us

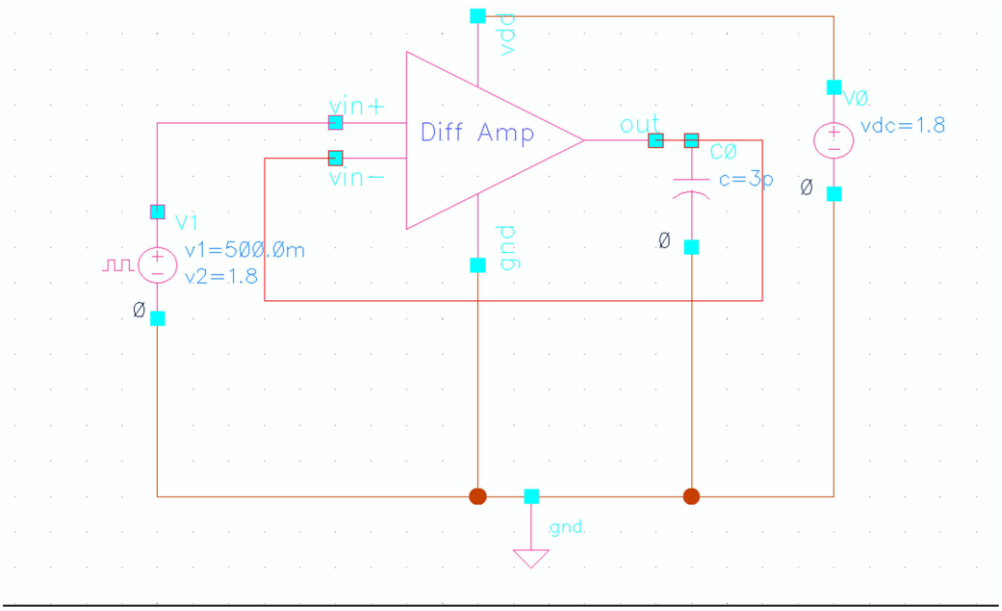

Figure 8: test setup to calculate slew rate

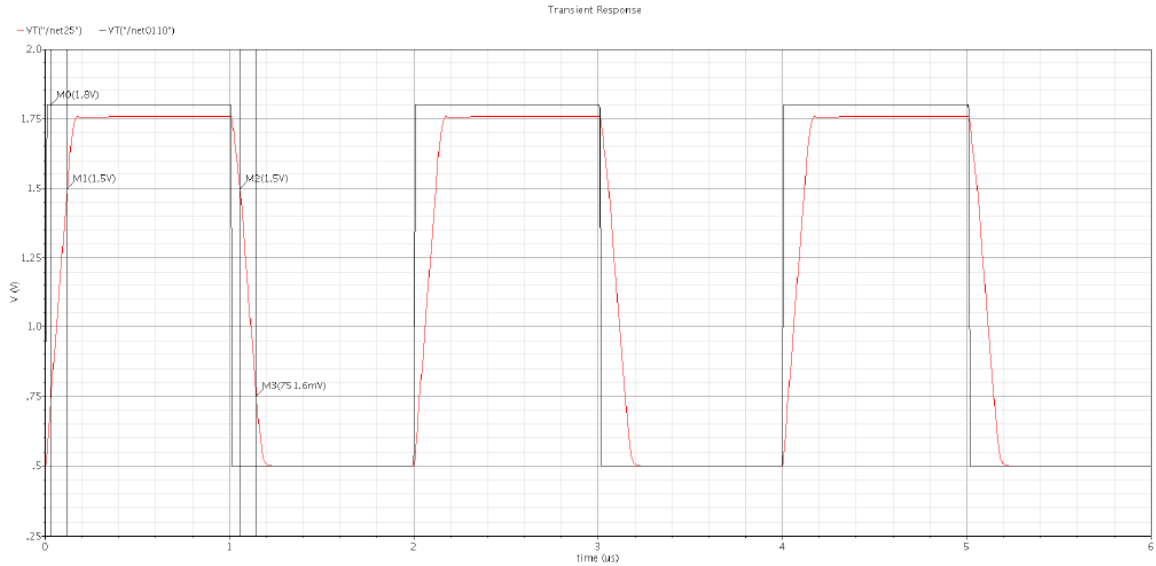

Figure 9: Operational amplifier Transient response

8. Conclusion

The following table shows the specifications that we achieved and its comparison with the required specifications.

	Avd	OVSR	SR	CMRR	GBW	PM	Power Dissipation
Required	85dB	1.4V	10V/us	80dB	8MHz	60deg	0.35mW
Achieved	79.05dB	1.41V	8.41V/us	128.05dB	15.43MHz	61.4deg	0.277mW
Marks	13.95	10	8.41	10	20	10	15

The design of operational amplifiers remains a cornerstone of analog electronics, enabling a wide range of applications in signal processing, data conversion, and control systems. This paper highlights the key principles and methodologies involved in developing high-performance op-amps, focusing on critical metrics such as gain, bandwidth, noise, and power efficiency. Advances in CMOS technology and optimization techniques, such as Quantum-Behaved Particle Swarm Optimization (QPSO), have significantly enhanced the precision and efficiency of modern designs [8].

Low-power and low-noise op-amps are crucial for portable and precision instrumentation, where innovations like rail-to-rail input stages and class-AB biasing ensure optimal performance. Validation through simulation and experimental testing ensures that these designs meet stringent application requirements [9].

In conclusion, operational amplifier design is a dynamic and evolving field, driven by advancements in technology and application demands. Future innovations will continue to push the boundaries of performance, integration, and energy efficiency, addressing the ever-growing needs of modern electronics.

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