

Comparison of 15, 21, 41 Level Cascaded H Bridge Multilevel Inverters with Reduced Number of Switches

**D. Adinarayana Naik¹, Shaik Adil Bokaree², Jaladi Venkata Gayathri³,
BonuSiva Ganesh⁴, Rayapudi Mohan Narayana⁵, Mellaka Raju⁶**

¹Assistant Professor, Electrical and Electronics Engineering, University College of Engineering, Narsaraopet, JNTUK, Andhra Pradesh, India

^{2,3,4,5,6}Student, Electrical and Electronics Engineering, University College of Engineering, Narsaraopet, JNTUK, Andhra Pradesh, India

Abstract:

Cascaded H-bridge multilevel inverters have been developed for applications including user interface of renewable energy, voltage regulation, VAR compensation, and harmonic filtering in power systems. A modified cascaded H-bridge multilevel inverter (MLI) is implemented for solar applications. Multilevel inverter based on cascaded H-bridge topology will help in the reduction in number of switches. This concept helps to reduce the complexity of switching compared to other multilevel inverters. In this paper, cascaded H-bridge multilevel inverters output is validated with a combination of RLC load. With the increase of the levels of inverter the total harmonic distortion will be reduced.

Keywords: CHB(Cascaded H Bridge), MLI (Multilevel Inverter), THD(Total Harmonic Distortion)

1. INTRODUCTION

Multilevel inverters (MLIs) belong to the family of converters that have immense potential in research and development. They have a wide range of applications in the power engineering sector. Areas of the applications include variable speed drives, Renewable Energy Systems (RES), HV direct current (HVDC) Transmission, flexible alternating current transmission systems (FACTS), and also electric vehicles (EVs) and More Electric Aircraft (MEA) systems. Now-a days, power generation using renewable energy resources has been increasing rapidly due to the fast depletion of fossil fuel and their worst impact on the environment. Proper synchronization is the key factor that is followed after the integration of multiple renewable generation units. To connect to the grid an AC voltage is required which is obtained by connecting an inverter in case of solar PV system, as the generation is DC voltage. Harmonics are the pollutant factors that affect the output from the inverter which collapses the power system. Thus a proper design of inverter with reduced harmonic distortion is considerably mandate.

Usually, a pure sine wave inverter doesn't exist in the world. So alternative and the near best option is modified sine wave inverters. In that, multilevel inverters(MLIs) are known for much economical, reliable and high efficient devices than other types. So, presently multilevel inverters have become common place because of their ability in voltage operation and function. The multilevel inverter gives the required output by using a number of independent DC voltage sources. The voltage output waveform of the inverter is obtained almost sinusoidal with increase in number of sources by using the

switching frequency. It shows low switching losses and low voltage stress because of several dc sources. The word multilevel starts with a three-level inverter. Multilevel inverters are gaining popularity in power electronic applications because they are well suited to handle the increased need for power rating and power quality associated with fewer switches and lower electromagnetic interference. In high switching frequency pulse width modulation (PWM), of multilevel inverters has several advantages over a conventional two-level inverter. When compared to 2-level inverters, MLIs produce better sinusoidal output reducing the Total Harmonic Distortion (THD), thus lowering filter requirements while also possessing higher efficiency, modularity, and reduced stress across power electronic devices. The three classical topologies of MLIs proposed in the literature are the flying capacitor (FC) MLI, neutral point clamped (NPC) MLI, and cascaded H-bridge (CHB) MLI, with each having several variants. The NPC topology has the problem of requiring a sizeable number of clamping diodes with greater levels forming output voltage waveform. FC MLI creates the problem of capacitor voltage balancing and proves to be expensive and unreliable for an increasing number of levels produced demanding a substantial number of capacitors. CHB MLI is unique in employing multiple dc sources, which gives modularity, compatible with being fed through a battery, solar PV module, or fuel cell. CHB MLI has lesser diodes and capacitor requirements when compared to the other classical topologies.

2. LITERATURE SURVEY

In paper [1], A three level and five level cascaded H bridge MLI is analysed and compared. As compared to neutral point clamped multilevel inverter and flying capacitor multilevel inverter, the cascaded H-Bridge multilevel inverters requires less number of components and it reaches high quality output voltage which is close to sinewave. The cascaded H-Bridge multilevel inverter are the most advanced and important method of power electronic converters that analyses output voltage with number of dc sources as inputs. Generally MLI is used for dc to ac power conversions and the simulation of multi-level inverter is done in MATLAB\SIMULINK. The THD(total harmonic distortion) is analysed and compared obtained in the output voltages of three-level and five level- cascaded H-bridge MLI. The THD in five-level cascaded multilevel inverter is less than the three-level cascaded multilevel inverter.

In paper[2], A 15-Level Asymmetric Cascaded H-Bridge Multilevel Inverter with a low number of switches For Photo Voltaic System is designed. In this paper Asymmetric MLI is used. Generally, a symmetrical multi-level inverter the input dc source magnitudes are equal like 50vdc,50vdc,50vdc where as in asymmetrical multilevel inverter the magnitudes of dc sources are unequal like 50vdc,100vdc,200vdc. Switching pulse and PD PWM switching techniques are used. This is designed in MATLAB/SIMULINK software. And at the end their THD are compared.

In paper[3],A Conventional Single Phase 21-level Cascaded H-Bridge Multilevel Inverter and Single Phase 21 Level Multilevel Inverter with Reduced Switches are designed. In conventional cascaded H bridge Multi level inverter is constructed, in which this type of topology uses different input voltages are proposed and the H bridges are connected in the series. In Conventional Single Phase 21-level Cascaded H-Bridge Multilevel Inverter 20 switches and 5 sources are used. where Single Phase 21 Level Multilevel Inverter is constructed by using 8 IGBT switches, 4 separate DC sources and 8 power diodes. And this topology is designed in MATLAB/SIMULINK and the harmonic spectrum is obtained

In paper[4], A Fifteen Level Cascaded H-Bridge Multilevel Inverter with Space Vector PWM Technique with Reduced Number of Switches is constructed. Generally, multilevel inverter produces number of positive layer and negative layers by using large number of switches which may leads to increase cost and size. In order to reduce the cost and size of equipment a new multilevel inverter is proposed with space vector PWM Technique and this technique reduce the number of switches and gets better performance. The scheme is developed in MATLAB/SIMULINK. And this proposed method reduces the switching losses and THD(Total Harmonic Distortion)

In paper[5],A 7-Level and 31-Level Cascaded H-Bridge Multilevel Inverters with Reduced Number of Semiconductor Switches is implemented in different topologies. A 7-level cascaded H-bridge multilevel inverter is symmetrical in nature whereas 31-Level Cascaded H-Bridge Multilevel Inverters is asymmetrical in nature. The PD-PWM modulation technique was used here to achieve switching sequence. The whole topology is simulated in the MATLAB/SIMULINK software. As increase in number of levels the THD(Total Harmonic Distortion) also decreases. So, the THD(Total Harmonic Distortion) in 31-level cascaded H-bridge multi-level has less compared to the 7-level cascaded multi-level inverter.

3. H-BRIDGE INVERTER

A simplified circuit diagram of a single-phase H-bridge inverter is shown in figure 3.1. It consists of two inverter legs,each of which has two MOSFETs. While the AC output voltage V_{ab} of an inverter can be changed using either bipolar or unipolar modulation approaches. The inverter's DC bus voltage V_d is typically fixed.

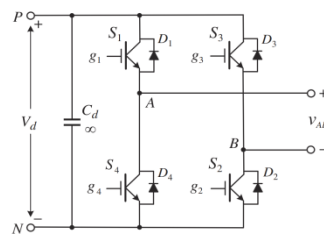


Figure3.1: Single-phase H-bridge inverter

4. CASCADED H BRIDGE TOPOLOGY FOR 15 LEVEL MULTI-LEVEL INVERTER

A 15 cascaded H-bridge asymmetrical multilevel inverter is a type of inverter that uses multiple H-bridge circuits connected in series, or "cascaded," to produce a higher number of voltage levels. The "asymmetrical" part of the name refers to the fact that the voltage levels produced by the inverter are not symmetrical around a midpoint, as they would be in a traditional inverter.

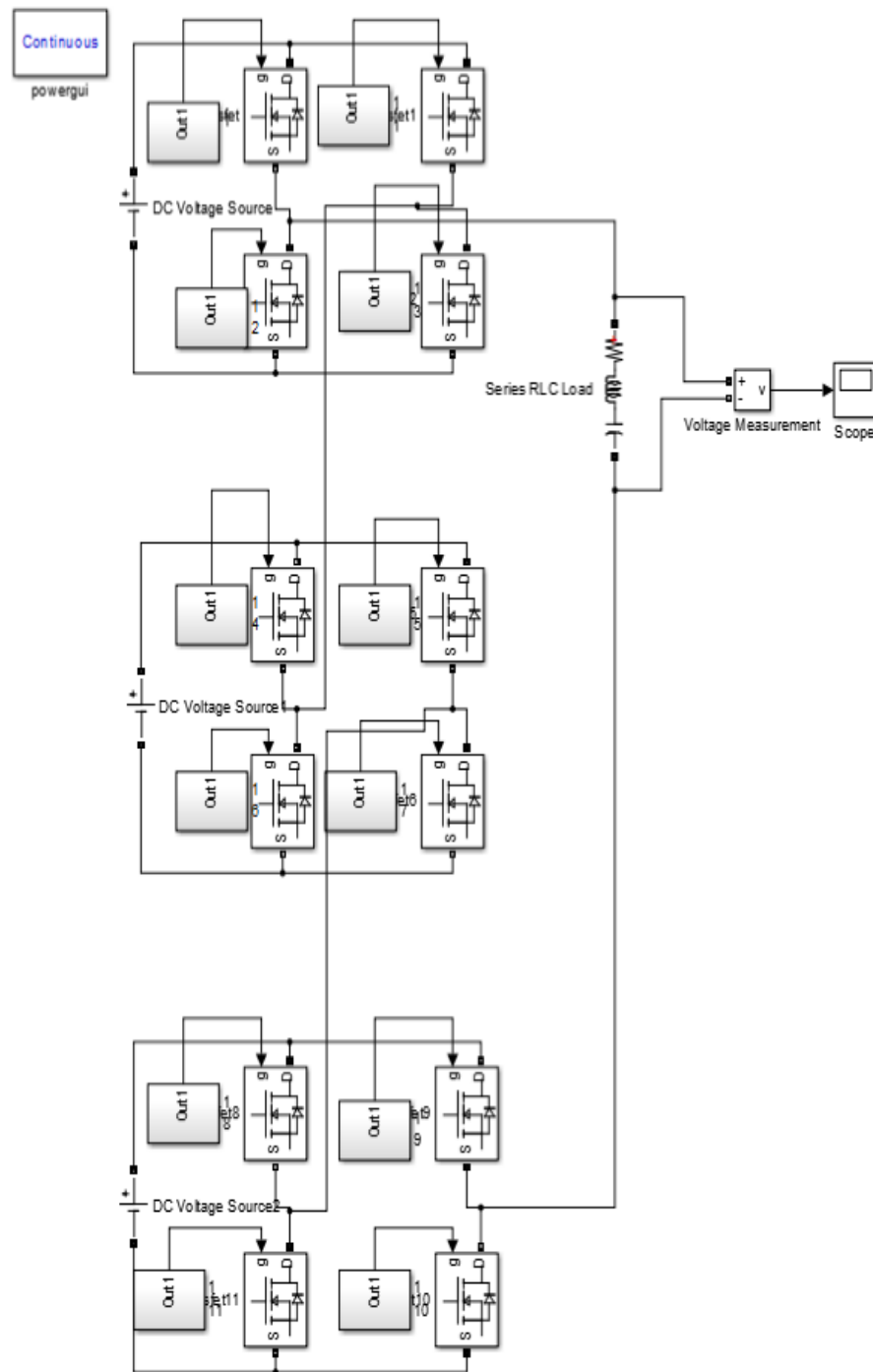


Figure 4.1: Circuit diagram for 15 level CHB-MLI

An H-bridge is a circuit configuration that allows for the direction of current flow through a load to be reversed by switching the polarity of the voltage applied to the load. By cascading multiple H-bridges together and controlling the individual switches in each one, a multilevel inverter can produce a much larger number of voltage levels than a traditional inverter.

In a 15 cascaded H-bridge asymmetrical multilevel inverter, there are 15 H-bridge circuits connected in series, which allows for a large number of voltage levels to be produced. The asymmetrical aspect of the inverter refers to the fact that the voltage levels produced will not be symmetrical around a midpoint, which can be useful in certain applications.

Table 4.1: Switching table for 15 level CHB-MLI

	0	5	10	15	20	25	30	35	30	25	20	15	10	5	0	-5	-10	-15	-20	-25	-30	-35	-30	-25	-20	-15	-10	-5
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
s1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0
s2	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
s3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1
s4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
s5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	1	0	0
s6	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
s7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	1	1	0
s8	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
s9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1
s10	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
s11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0
s12	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The above table is prepared by using certain formulae to get the values.

- Number of steps $2(N-1)$
- Phase delay = $(\text{period} / \text{total number of steps}) * \text{step}$
- Pulse width = $(\text{number of pulse width} / \text{total number of steps}) * 100$

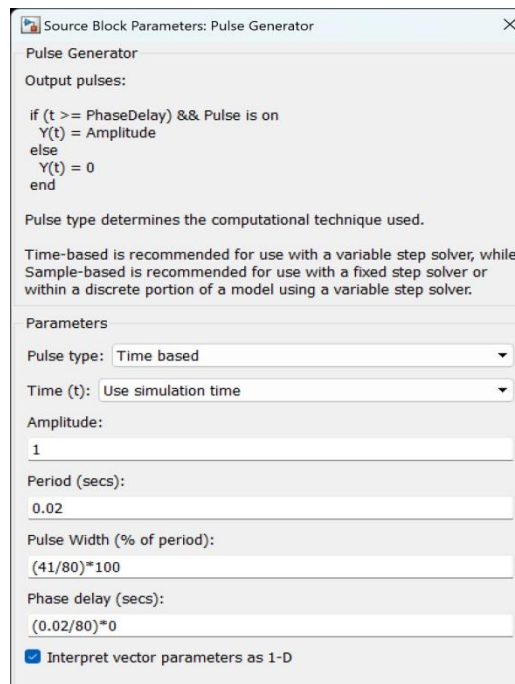


Figure 4.2: Block parameters of Pulse Generators

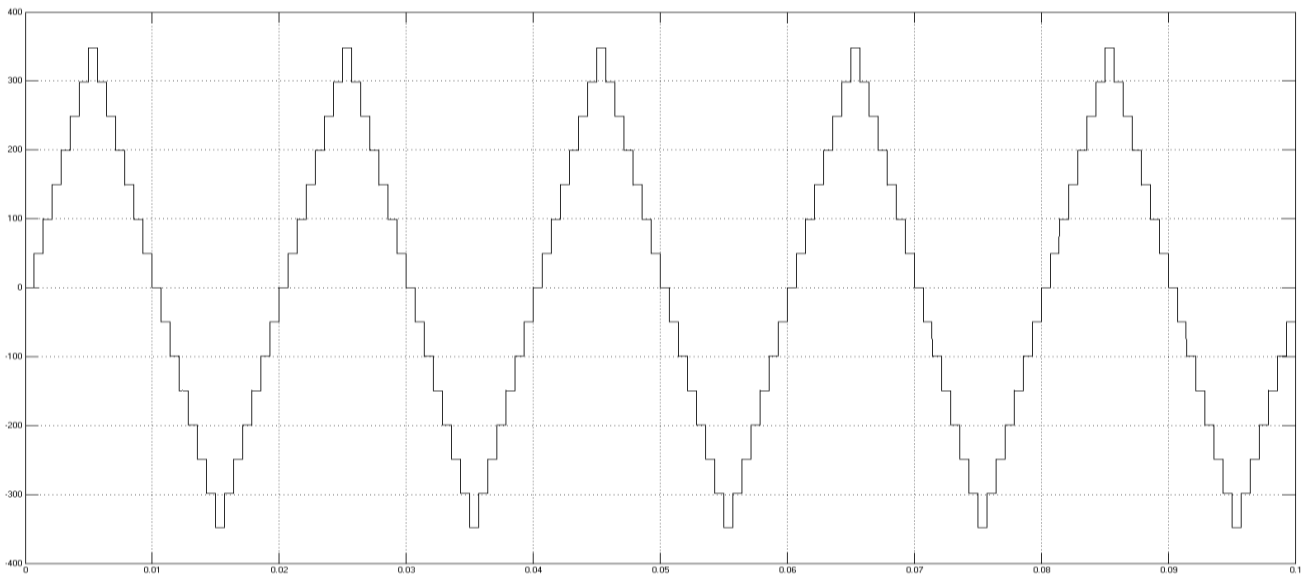


Figure 4.3: Simulation output of 15 level CHB MLI

5. CASCADED H BRIDGE TOPOLOGY FOR 21 LEVEL MULTI-LEVEL INVERTER

21 level asymmetrical MLI consists of 4 cells/modules of H-bridge. Each cell/module contains 4-MOSFETS. As it is asymmetrical it has four different dc sources of magnitude such as 10vdc, 20vdc, 30vdc, 40vdc. Each cell/module is connected in series passion. Different Loads are connected across the circuit like R load, RL load, RLC load as shown in figure 5.1 In MOSFET the Gate signal is given by the pulse generator, the switching technique is shown in switching table.

Table 5.1: Switching table for 21 level chb-ml

1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39									
2	0	10	20	30	40	50	60	70	80	90	100	90	80	70	60	50	40	30	20	10	0	-10	-20	-30	-40	-50	-60	-70	-80	-90	-100	-90	-80	-70	-60	-50	-40	-30	-20	-10									
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	0	1	0	1	0	1	1	0	1	1	0	1	1	1	0						
4	2	1	0	1	1	1	0	1	1	0	1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1					
5	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	0	1	0	0	0	1						
6	4	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
7	5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	0	1	1	0	0	1	1	0	1	1	1	1	0	1					
8	6	1	1	0	1	1	1	0	1	1	0	0	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
9	7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0				
10	8	0	0	1	0	0	0	1	0	0	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
11	9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
12	10	1	1	1	0	1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
13	11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
14	12	0	0	0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
15	13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
16	14	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
17	15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
18	16	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

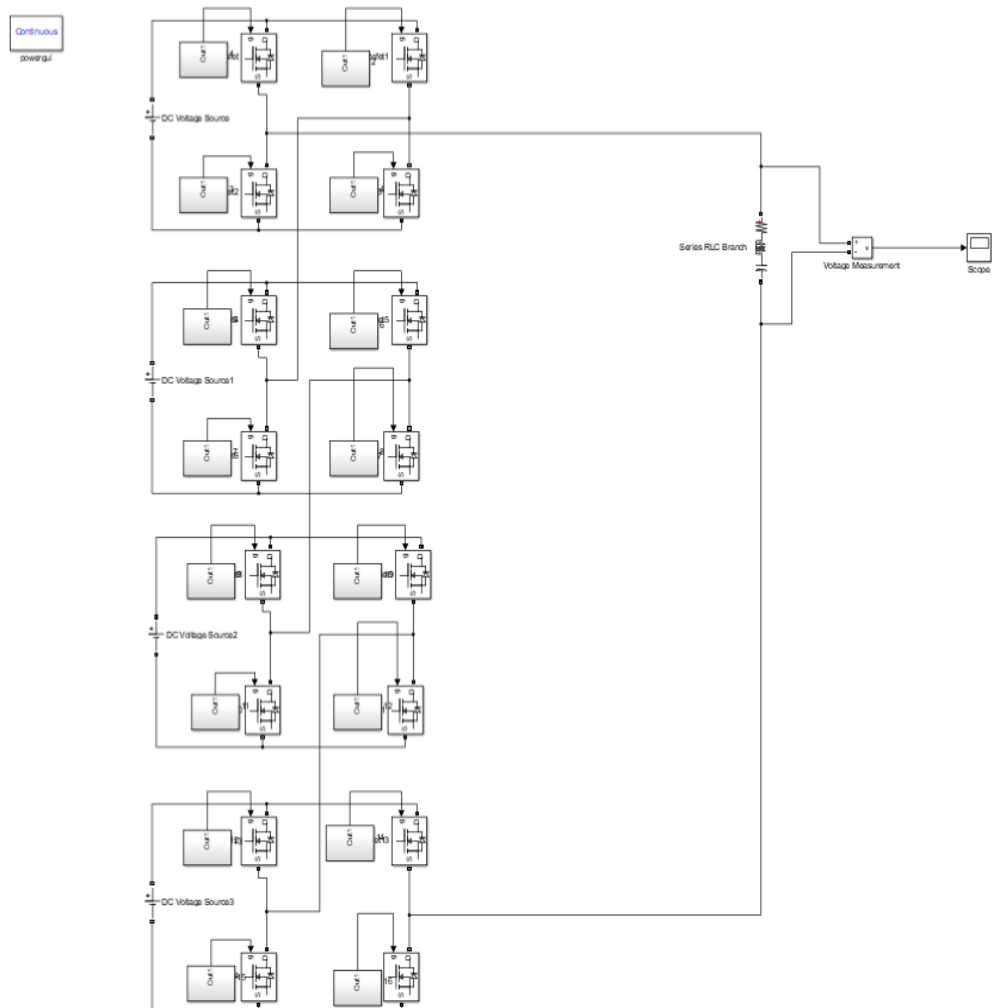


Figure 5.1: Circuit diagram for 21 level chb-mlt

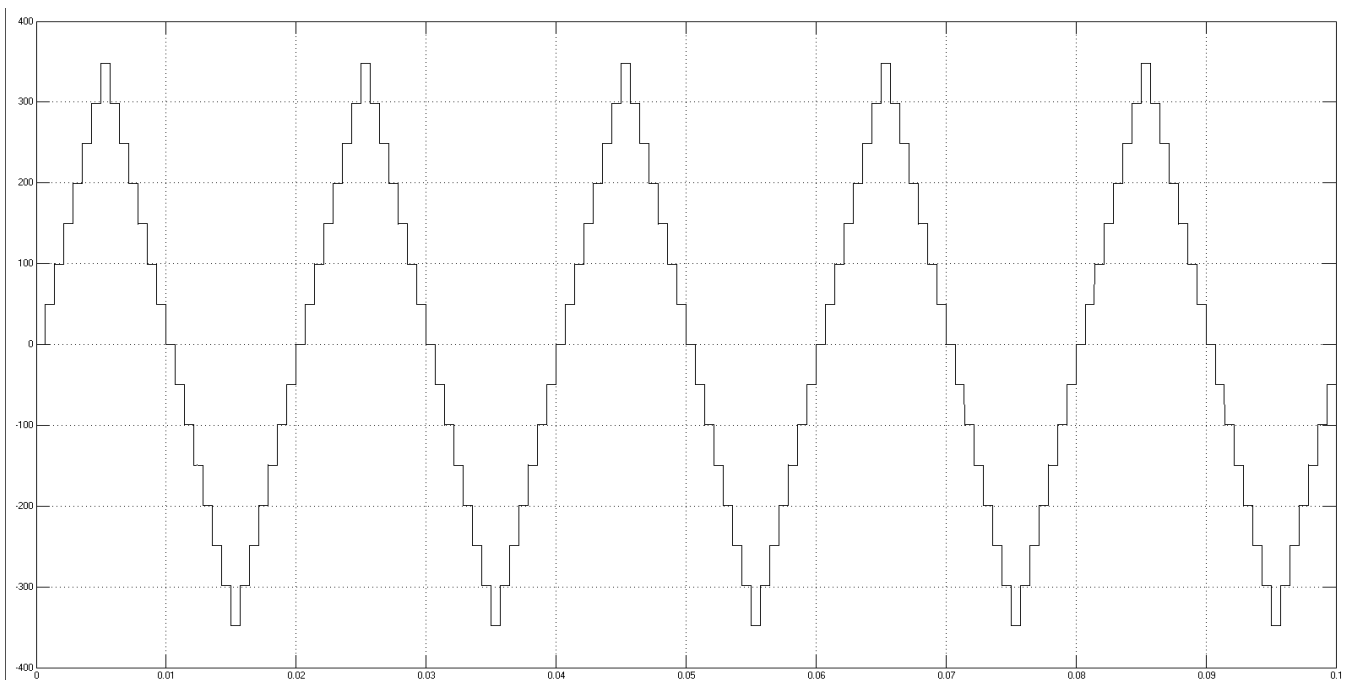


Figure 5.2: Simulation output of 21 level chb-mlt

6. CASCADED H BRIDGE TOPOLOGY FOR 41 LEVEL MULTI-LEVEL INVERTER

Similarly in 41 level cascaded H bridge multilevel inverter contains five cells/module, and they are connected in the series. And Loads are connected across the circuit as shown in figure. In this proposed system a cell contains four switches s_1, s_2, s_3 and s_4 within in which one combination of switches operate for positive half cycle i.e switch s_1 and s_3 , for operation of negative half cycle i.e s_2 and s_4 with five different dc sources 5v, 10v 15v 30v 40v. The circuit diagram for proposed topology is shown in figure 6.1

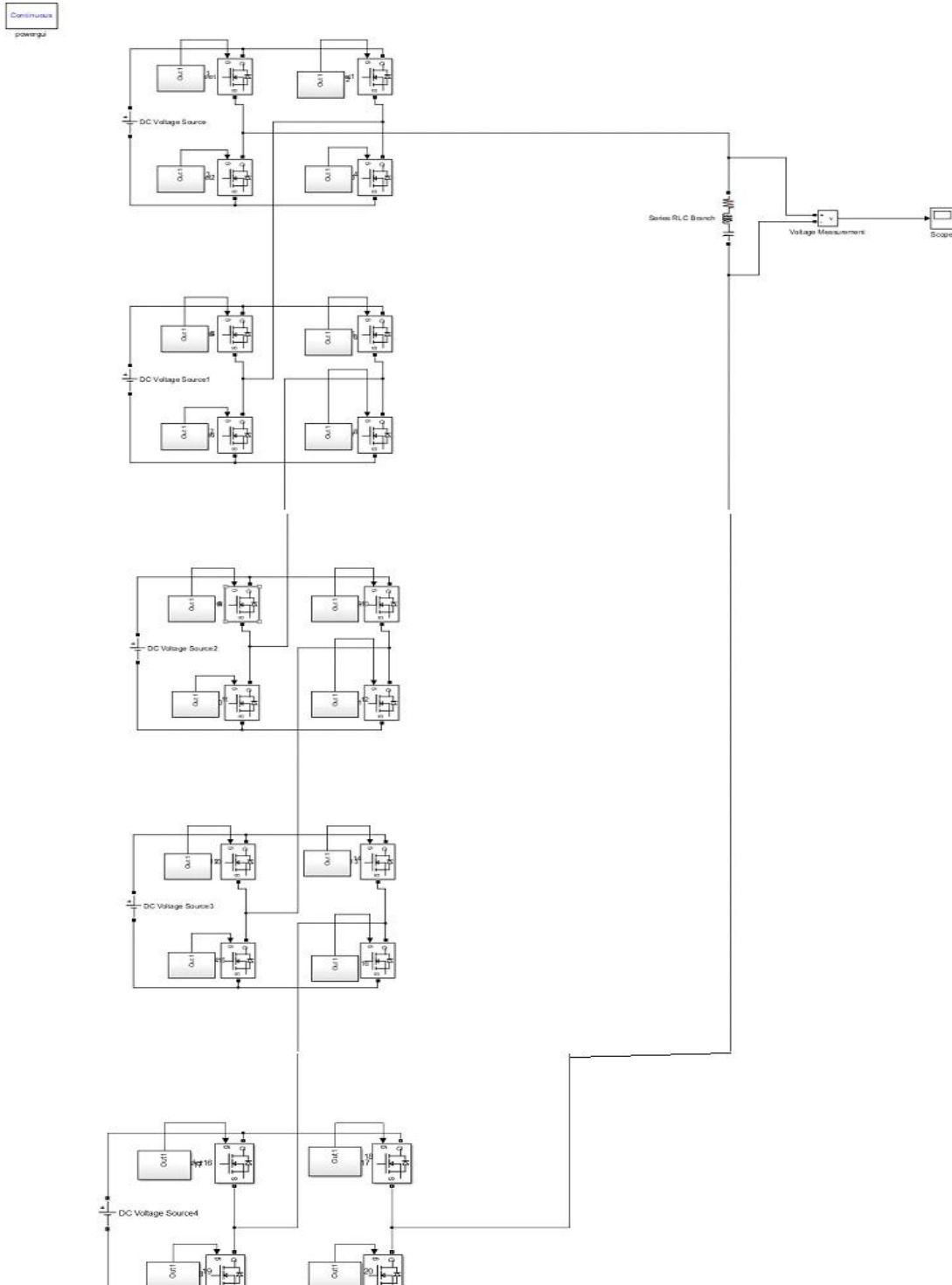


Figure 6.1: Circuit diagram for 41 level chb-ml

7. THD ANALYSIS OF 15-LEVEL, 21-LEVEL AND 41-LEVEL CHB MLIs

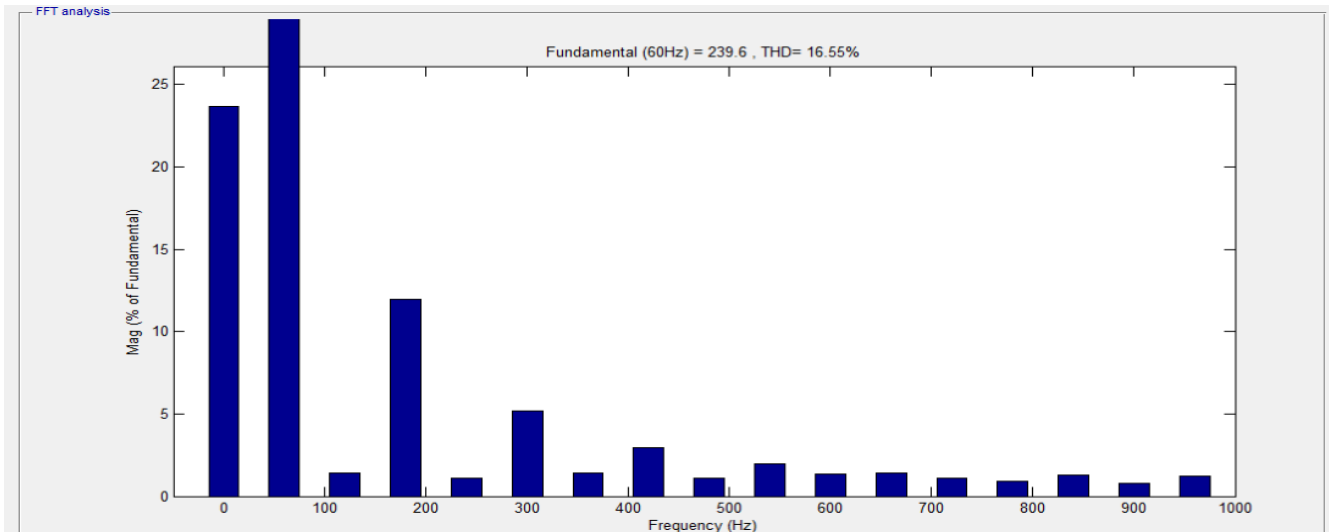


Figure 7.1 THD for level 15

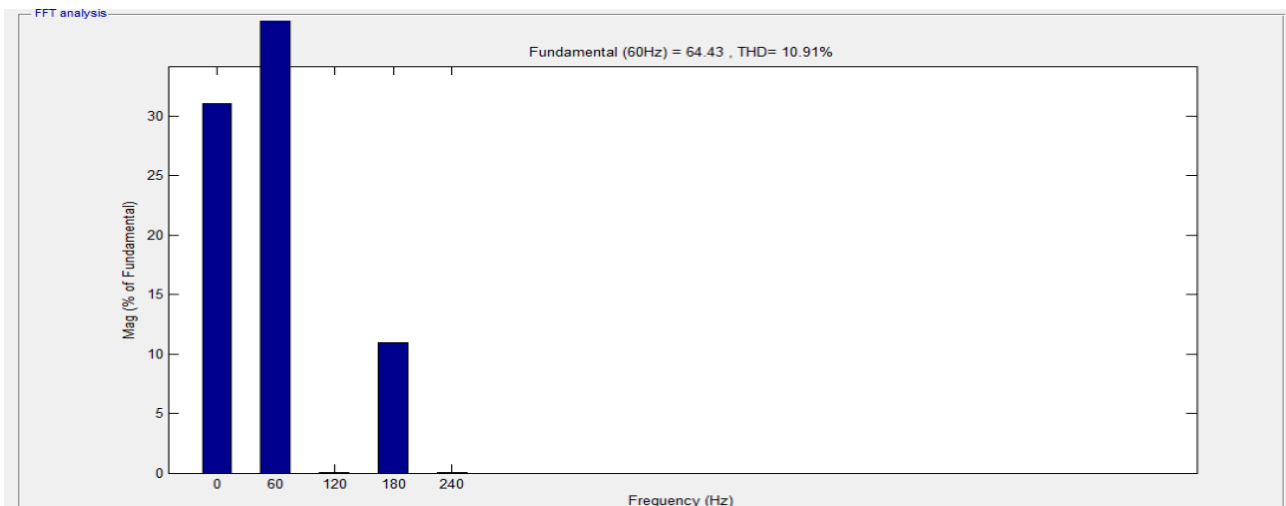


Figure 7.2: THD for level 21

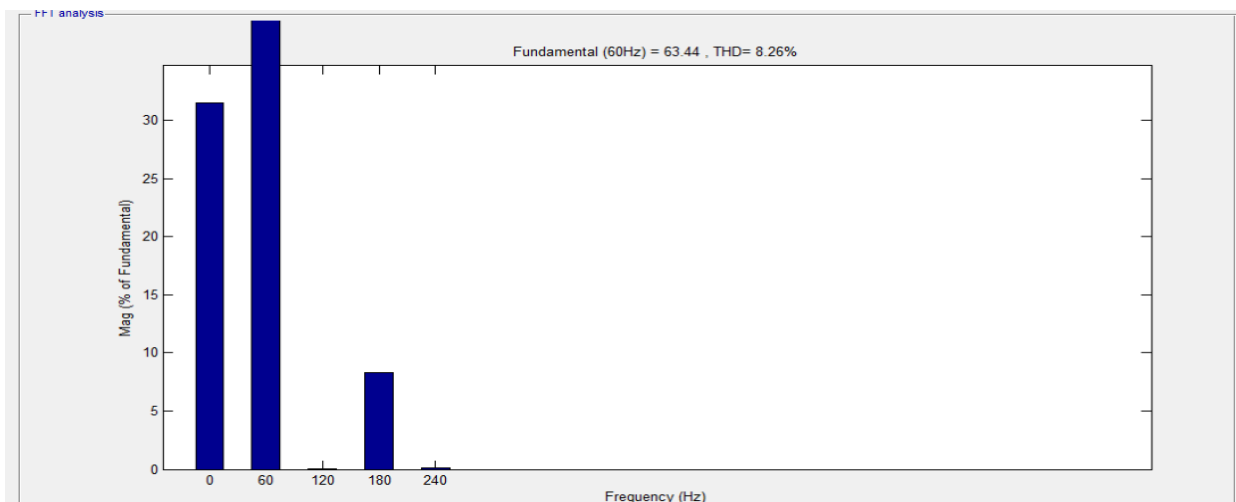


Figure 7.3: THD for 41 level CHB MLI

Table 7.1: Analysis of Cascaded H Bridge MLI for proposed levels

Multilevel inverter	No. of Semiconductor switches	THD%
15-level CHB MLI	12	16.55%
21-level CHB MLI	16	10.91%
41-level CHB MLI	20	8.26%

CONCLUSION

The CHB MLI for 15, 21 and 41 level multilevel inverter with minimized number of semiconductor switches by using pulse generators has been implemented. CHB MLI are used extensively because of their better quality output voltage waveforms as compared to other types of MLIs. This paper gives THD of 16.55% for 15-level CHB MLI, 10.91% for 21-level and 8.26% for 41-level CHB MLI and therefore the AC output waveform nearly looks like a sine wave for 41-level. The proposed inverters are used integration of Renewable Energy Sources, FACTS, HEVs, Power quality improvements.

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