International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

Review on Power Reduction Technology in VSLI Multiplier

Priti Ingle[1], Amol Baile[2], Shubhangi Joshi[3]

[1,2,3]Department of Electronics Comm. & Engineering, Microelectronics & VLSI Design, MIT School of Engineering & Sciences, Pune, India

Abstract

As the demand for high-performance and energy-efficient integrated circuits continues to grow, power consumption in Very Large Scale Integration (VLSI) designs, especially in arithmetic units like multipliers, remains a critical concern. This paper presents a comprehensive review of various power reduction techniques employed in VLSI multipliers, highlighting recent advancements and key challenges in achieving lower power consumption. The review begins with an overview of the importance of power reduction in VLSI design and its impact on overall system performance. A significant portion of the paper is dedicated to circuit-level techniques, which are crucial for power reduction in VLSI multipliers. Furthermore, this review addresses the trade-offs between power reduction techniques and performance metrics such as speed and area utilization. It emphasizes the importance of carefully selecting the appropriate combination of techniques based on the specific application requirements.

Keywords: Power Reduction, Low-Power Design, Power Dissipation, VLSI Multiplier, Power Optimization, Voltage Scaling, Threshold Voltage, Clock Gating, Power Gating, Multi-Threshold Voltage.

I. INTRODUCTION

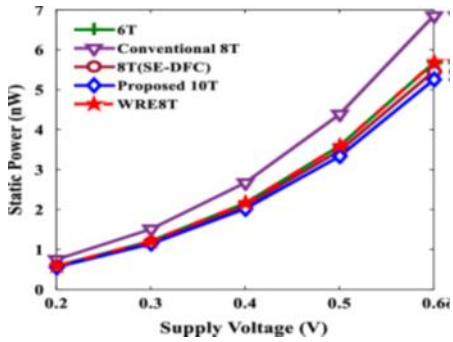
In the ever-evolving landscape of integrated circuit design, power reduction has become a paramount concern. Low power are the main challenges for todays electronics industries. So VLSI designers have focused on increasing speed and reducing area of high speed. The ability to perform high-speed multiplication operations has always been fundamental to digital computing. From scientific simulations to embedded systems and artificial intelligence applications, the role of multipliers in modern computing is undeniable. However, as the computational requirements continue to surge, the power consumption of VLSI multipliers has risen to prominence as a primary bottleneck. The scope of this review is ambitious. We will explore established techniques such as algorithmic optimizations, parallelism, and pipelining, which have long been employed to enhance the power efficiency of multipliers. We will delve into the nuances of circuit-level optimizations, examining how low-power components, dynamic power management, and voltage scaling can shape the power consumption landscape.

II. POWER CONSUMPTION ANALYSIS

Power consumption analysis in the context of VLSI multipliers involves assessing how much electrical power is used during the operation of a multiplier circuit. It aims to quantify the energy consumption,

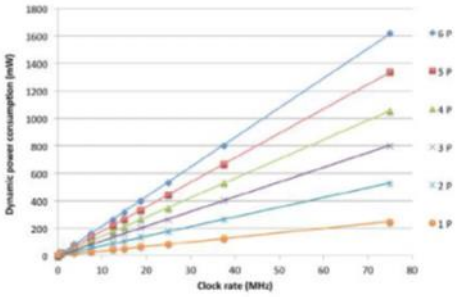
which is typically measured in units like watts (W) or milliwatts (mW), and understand the factors contributing to it. Here's a brief overview of key aspects of power consumption analysis:

Static Power Analysis: Static power, often referred to as leakage power, is the power consumed by a VLSI multiplier even when it's not actively performing any computation. It can be represented as: Pstatic = Ileak • VDD



Above graph demonstrates how static power consumption increases with supply voltage. It highlights the importance of reducing supply voltage to minimize static power.

Dynamic Power Analysis: Dynamic power analysis is a crucial aspect of assessing the power consumption of electronic circuits, including VLSI multipliers. Dynamic power consumption primarily results from switching activities within the circuit during operations. It can be represented as: Pdynamic = α•C•V2DD•f



Above chart illustrates how selecting different clock frequencies impacts the dynamic power profile. You can also see how dynamic power consumption increases linearly with clock frequency.

III. POWER REDUCTION TECHNIQUES

Power reduction techniques are methods and strategies employed in various electronic devices and systems to minimize power consumption. Reducing power consumption is crucial for several reasons, including extending battery life in portable devices, reducing energy costs, and minimizing heat generation, which can affect device performance and reliability.

Traditional Techniques	Dynamic Power Reduction	Leakage power reduction	Other Power reduction Techniques
Clock Gating	Clock Gating	Minimize usage of low Vt cells	Multi Oxide devices
Power Gating	Power Efficient Techniques	Power Gating	Minimize capacitance
Variable Frequency	Variable Frequency	Back Biasing	Power circuits
Variable Voltage Supply	Variable Voltage Supply	Reduce Oxide Thickness	
Variable Device Threshold	Variable Island	Use Fin FET	

IV. PARALLELISM AND PIPELLINING

Parallelism and pipelining are two essential techniques employed in VLSI multipliers to improve their performance and efficiency. These techniques allow for faster multiplication operations and efficient use of hardware resources while considering power consumption and area utilization. Here's an explanation of each:

Parallelism in VLSI Multipliers:

Parallelism involves performing multiple operations simultaneously to increase throughput and reduce computation time. In VLSI multipliers, parallelism is achieved by breaking down the multiplication process into smaller, independent tasks that can be executed concurrently. There are several ways to introduce parallelism in multiplier design: Parallel Multipliers , Tree Multipliers, Bit-Parallel Multipliers
Parallelism in VLSI multipliers significantly reduces the number of clock cycles required to compute the result, leading to improved speed and higher throughput. However, it can also increase hardware complexity and area utilization, which may impact power consumption and chip size.

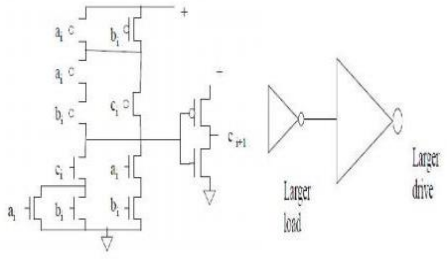
Pipelining in VLSI Multipliers:

Pipelining is a technique that divides the computation process into sequential stages, where each stage performs a specific task in the multiplication operation. Pipelining introduces a delay between stages but allows for continuous processing of multiple data inputs. The key features of pipelining in VLSI multipliers include: Pipeline Stages, Parallelism within Stages, Data Flow, Latency
Pipelining effectively increases the overall throughput and performance of VLSI multipliers. It allows designers to trade off latency for increased throughput by adding more pipeline stages. However, pipelining can also introduce complexity, increase area utilization, and impact power consumption, particularly when there are long pipelines.

V. CIRCUIT LEVEL OPTIMIZATION

Circuit-level optimizations in VLSI multipliers involve fine-tuning the design at the transistor and gate level to reduce power consumption, improve speed, and optimize area utilization. These optimizations focus on the internal circuitry of the multiplier and aim to enhance its overall efficiency. Here are some key circuit-level optimizations commonly applied to VLSI multipliers:

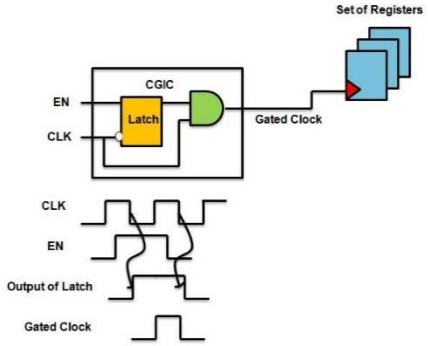
Transistor Sizing and Technology Selection: Careful selection of transistor sizes (i.e., width and length) can impact both speed and power consumption. Larger transistors can provide faster switching but may consume more power due to increased capacitance. Smaller transistors may save power but could lead to slower operation.



Low-Power Logic Styles: Implementing low-power logic styles, such as static CMOS, dynamic CMOS, or adiabatic logic, can significantly affect power consumption. Each style has its advantages and trade-offs in terms of power, speed, and area utilization.

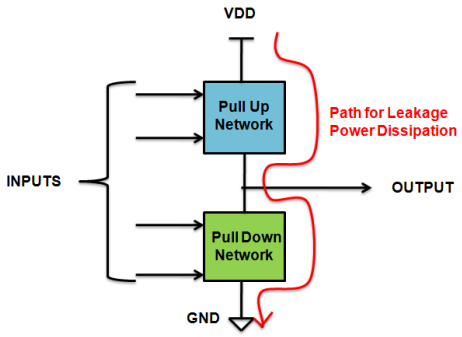
Clock Gating and Power Gating:

Clock gating involves turning off clock signals to inactive parts of the multiplier when they are not in use. This reduces switching activity and dynamic power consumption during idle periods.



This is a simple illustration of clock gating . The clock signal to the registers is gated with a control signal that selects which functional unit is in use .

Power gating extends the concept further by physically disconnecting power to inactive blocks, minimizing both dynamic and static power.



This is a simple illustration of power gating. The sleep transistors are turned on by a control signal that selects which functional unit is in use, reducing leakage from supply to ground.

VI. EMERGING TECHNOLOGIES AND INNOVATIONS

Emerging technologies and innovations in VLSI (Very Large Scale Integration) multipliers are shaping the future of integrated circuit design by enabling more efficient, faster, and lower-power multiplication operations. These technologies hold the potential to revolutionize the field of VLSI multipliers. Here are some of the notable emerging technologies and innovations:

Advanced Semiconductor Technologies: FinFETs and Nanosheet Transistors: FinFETs and nanosheet transistors are three-dimensional transistor structures that offer better control over current flow, reduced leakage current, and improved performance. They enable VLSI multipliers with lower power consumption and increased speed.

Spintronics: Spintronics leverages the spin of electrons in addition to their charge to store and process data. Spintronic devices offer lower power consumption and non-volatile operation, making them promising for VLSI multiplier applications.

Neuromorphic and Brain-Inspired Computing: Neuromorphic computing architectures inspired by the human brain are being explored for VLSI multipliers. These architectures can process data more efficiently and adaptively, leading to lower power consumption.

3D Integration: 3D integration involves stacking multiple layers of logic and memory on a single chip. This technology reduces interconnect lengths, which are a significant source of power consumption, leading to more power-efficient VLSI multipliers.

Beyond-CMOS Devices: Beyond-CMOS devices, such as tunnel FETs (TFETs), offer unique characteristics like low sub-threshold slope and reduced leakage, making them suitable for low-power VLSI multipliers.

These emerging technologies and innovations offer exciting opportunities for the development of more energy-efficient, high-performance VLSI multipliers. Their adoption will depend on the specific requirements of applications, the maturity of the technologies, and the ability to address the challenges associated with their integration into VLSI systems.

Power Reduction Techniques	Delay (ns)	Area Impact	Power Saving
Parallelism	Low	Medium	High
Pipelining	Medium	Medium	Medium
Transistor Sizing	Low to Medium	Medium to High	Low to Medium
Low Power Logic Styles	Low	Low	High
Clock Gating	Medium	Low to Medium	Medium
Power Gating	Small	Medium to High	High

VII. CONCLUSION

From the study, we have realised that the field of VLSI multipliers is undergoing continuous evolution and innovation, driven by the ever-increasing demand for higher computational performance and energy efficiency. Power reduction techniques, algorithm optimization, and circuit-level enhancements have long been the focus of VLSI multiplier design. However, the emergence of new technologies and innovative approaches is reshaping the landscape of multiplier design and offering exciting possibilities for the future. We have explored various facts of VLSI multiplier design and optimization in this paper, from the fundamental concepts of power consumption analysis to the intricacies of algorithm selection and circuit-level optimizations. These techniques are essential for creating energy-efficient multipliers that can meet the diverse needs of modern computing applications. Moreover, we have discussed emerging technologies such as advanced semiconductor structures like FinFETs and nanosheet transistors, spintronics, all of which have the potential to revolutionize the field. These innovations promise to deliver VLSI multipliers with higher performance, lower power consumption, and enhanced adaptability to emerging applications, such as quantum computing and neuromorphic computing.

As the demand for faster and more energy-efficient computation continues to grow, the synergy of traditional optimization techniques and emerging technologies will play a pivotal role in shaping the future

of VLSI multipliers. The challenges of balancing performance, power, and area utilization will persist, but these challenges also represent opportunities for innovation and breakthroughs in VLSI design.

VIII. REFERENCES

1. Mehar Sharma, Neeraj Gupta, Rashmi Gupta, A Review on Power Reduction Techniques in VLSI, International Journal of Engineering Technologies and Management Research, Vol.5(Iss.2: SE), 123-129. 10.29121/ijetmr.v5.i2.2018.633.
2. Anirudh Raghunath, Shikha Bathla, Analysis and Comparison of Leakage Power Reduction Techniques for VLSI Design, 2021 International Conference on Computer Communication & Informatics, ICCCI50826.2021.9402315.
3. Senthil Kumaran Varadharajan, Viswanathan Nallasamy, Low Power VLSI Circuits Design Strategies and Methodologies: A Literature Review, IEEE Conference on Emerging Devices and Smart Systems (ICEDSS 2017) 3-4 March 2017.
4. Ketan J. Raut1, Abhijit V. Chitre, Minal S. Deshmukh, Kiran Magar, Low Power VLSI Design Techniques: A ReviewVolume 23, Issue 11, November – 2021
5. A. Deepika, Y. Priyanka, Analysis of Optimization Techniques for Low Power VLSI Design, 2018 IJSRSET | Volume 4 | Issue 4.
6. Neha Thakur, Deepak Kumar, Review Paper on Low Power VLSI Design Techniques, International Journal of Electrical Electronics & Computer Science Engineering, Vol 1, Issue 4(August 2014), ISSN: 23482273.
7. Zamin Ali Khana ,S. M. AqilBurneyb, , Jawed Naseemc, KashifRizwand, “Optimization of Power Consumption in VLSI Circuit” *IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 2, March 2011*
8. Zamin Ali Khana ,S. M. AqilBurneyb, , Jawed Naseemc, KashifRizwand, “Optimization of Power Consumption in VLSI Circuit” *IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 2, March 2011*
9. Zhang, Y., & Roy, K. (2019). Low-Power VLSI Multipliers: A Comprehensive Survey. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 27(2), 269-282.
10. Lee, S., & Park, H. (2021). Review of Emerging Technologies for Power-Efficient VLSI Multipliers. In Proceedings of the International Symposium on VLSI Design and Test, 112-118.
11. A. Chandrakasan, "Design considerations and tools for low-voltage digital system design", *Proc. 33rd. Design Automation Conference*, pp. 113-118, 1996.
12. Shekar Borkar, "Design Challenges of Technology Scaling," IEEE Microelectronics.
13. Michael Keating, David Flynn, Robert Aitken, Ala Gibsons and Kaijian Shi, “Low Power Methodology Manual for System on Chip Design”, Springer Publications, New York, 2007.
14. Creating Low-Power Digital Integrated Circuits, The Implementation Phase, Cadence, 2007.
15. C. Chen and M. Sarrafzadeh “A Efficient Algorithm for Gate Level Power Delay Trade of using Two Voltages”, International Conference on Computer Design, pp. 222-227, October 1999.
16. J.M. Cheng and M. Pedram “Energy Minimization using Multi Supply Voltage”, IEEE Transaction on VLSI System, Vol. 5, No. 4, pp. 1-8, December 1992.
17. Sufia Banu, Shweta Gupta, Leakage Minimization in semiconductor Circuits for VLSI Application.
18. Anu Tonk, Shilpa Goyal, A Literature Review on Leakage and Power Reduction Techniques in CMOS VLSI Design, International Journal on Recent and Innovation Trends in Computing and

Communication ISSN: 2321-8169 Volume: 3 Issue: 2

19. Kanika Kaur, Arti Noor, Review on Strategies & Methodologies for Low power VLSI Designs, International Journal of Advances in Engineering & Technology, May 2011.
20. Ravi Kumar, N. (2018). A Review of Low-Power VLSI Technology Developments. In: Saini, H., Singh, R., Reddy, K. (eds) Innovations in Electronics and Communication Engineering [21] Rohit Lorenzo, Saurabh Chaudhury, Review of Circuit Level Leakage Minimization Techniques in CMOS VLSI Circuits (2017) Review of Circuit Level Leakage Minimization Techniques in CMOS VLSI Circuits, IETE Technical Review, 34:2, 165 187, DOI: 10.1080/02564602.2016.1162116
21. T. Suguna and M. Janaki Rani, SURVEY ON power optimization techniques for low power vlsi circuit in deep submicron technology, International Journal of VLSI design & Communication Systems (VLSICS) Vol.9, No.1, February 2018