

# Novel Architecture of FIR Lattice Filter with Reduced Interconnect Delay Impacts Towards Reduced Power-Delay Product Using Pipelining and Parallel Processing for Medical Applications

S. Subathradevi<sup>1</sup>, C. Vennila<sup>2</sup>

<sup>1</sup>Assistant Professor, Department of ECE, Anna University, BIT Campus, Tiruchirappalli, TamilNadu, India

<sup>2</sup>Professor, Department of ECE, <sup>2</sup>Saranthan College of Engineering, Tiruchirappalli, TamilNadu, India

## Abstract

Three important parameters area, speed and power are important. In VLSI design, the speed is determined by the critical path delay. Delay is depending on the data path taken for processing in the VLSI design. By minimizing data-path delay using efficient architecture the speed of the design of system can be improved in turn to result in better performance. In this new era, data-path delay is the dominating one compared to logic delay. So, it is very essential to concentrate more towards path delay in any architecture design. Even though the speed is important it is having in trade of with power. This data-path delay can be reduced by different technique like pipelining, parallel processing, register retiming. Also, by constructing this architecture in an innovative way the power is having trade of with delay. So the power-delay product can be taken as the reduced one. In this paper, various architecture of delay-product optimized FIR filter and Lattice filter architecture is being surveyed and implemented in order to get minimum delay-power product.

**Keywords:** VLSI, Architecture, FIR filter, Lattice filter, delay, path delay, pipelining, parallel processing, System design.

## I-INTRODUCTION

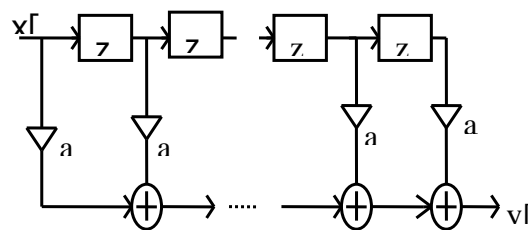
Finite impulse response (FIR) digital filters are common components in many digital signals processing (DSP) system. Throughout the years, with the increasing development in very large scale

Integration (VLSI) technology, the real time realization of FIR filter with less hardware requirement and less latency has become more and more important. The delay constrain is being met by the number of adder and multiplier used in the architecture and the way how they are interconnected to result with the longest path. So, in any system design, the arithmetic units are as much important to make it as a successful design. In arithmetic unit adders took much more contribution to play a role since subtraction and multiplication are all computed by addition and subtraction computation. So, if the speed is achieved by minimizing the delay in the architecture of adder and multiplier surely it leads to better performance in the speed of the design in the system.

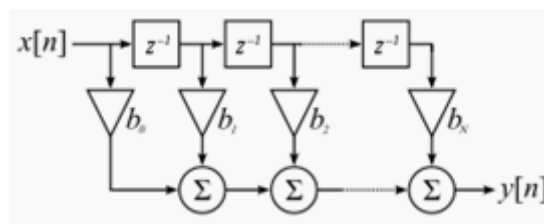
So, various array multiplier architectures are realized and their delay is compared. As the complexity of implementation increases with the length of filter, several algorithms have been mapped into effective architectures using ASIC and FPGA, where one of them is being the distributed arithmetic.

In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to to any finite length input) is of finite duration, because it settles to zero in finite time.

This is in contrast to infinite impulse response (IIR) filters, which may have internal feedback and may continue to respond indefinitely. The impulse response of an N-th order discrete-time FIR filter lasts exactly N+1 samples before it then settles to zero. FIR filters can be discrete-time or continues time, and digital or analog.

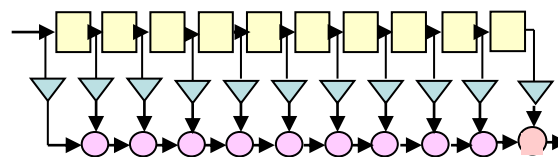


**Fig.1 N-tap FIR Filter**

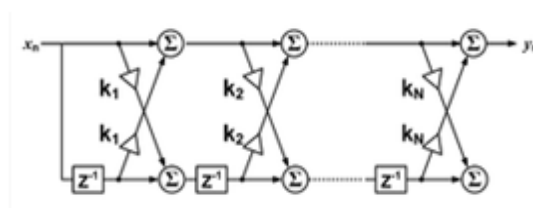


**Fig.2 4-tap FIR Filter**

The flow of the paper is organized in the following way as, Section - I gives about the Introduction. Section - II gives out the details about FIR filter. Section - III deals with Literature Survey on the FIR filter architecture used for delay reduction and Section -IV narrates conclusion and discussion.



**Fig.3 dfg of 11-Tap Filter**



**Fig.4 Lattice form Discrete time filter**

Matrix models ensure that medicine prescribing is founded upon multiple rational and evidence-based criteria; other non-rational selection criteria do not play a role in the decision-making process. As a result, medicine prescribing becomes transparent and reproducible as the criteria and weightings on which decisions are based are known. A matrix which involves multiplication and addition model also avoids the situation where a decision is taken solely on one criterion and therefore supports a comprehensive approach towards medicine prescribing. The use of matrix models in The Netherlands and Northern Ireland suggests that this method for medicine prescribing greatly aids discussion in pharmacotherapy audit meetings between general practitioners and/or pharmacists, local or regional formulary committees, pricing, and reimbursement negotiations.

### **III-LITERATURE SURVEY**

Various delay targeted architecture of FIR filter with their features is surveyed, compared and their contribution was viewed in connection with delay, which was briefed with various literature papers.

In paper [1], narrated that any FIR filter accuracy depends upon the filter coefficient, where low power and area efficient discrete wavelet transform architecture for fir filter is implemented. Whereas in paper [2] explained about the efficient design of FIR filter in order to reduce number of adders and multipliers and also the hardware complexity. For that different techniques and algorithms are used in that paper. In paper [3] FIR filter has been designed and realized by FPGA for filtering the digital signal. This implementation of FIR filter was done on cyclone IV GX FPGA. Today digital systems are designed by writing software in the form of HDL, the same was done on the paper.

In paper [4] it gives the basic structure and principles of FIR filter and give an efficient FIR filter on FPGA. Use MATLAB FDA tool to determine filter coefficients and designed to constant coefficient FIR filter by VHDL. The use of ISE 10.1 was used to simulate the performance of filter using two different techniques. The use of this software significantly shortens the R&D periods. The conclusion is windowing is better compared to frequency sampling.

In paper [5] it gives reduced dynamic power consumption of a digital filter which uses low power MUX based shift/add multiplier without clock pulse.

Glitching is also reduced. The proposed FIR filter has been synthesized and implemented using Xilinx ISE VT.1 and VIRTEX FPGA to target device XC4VLX200. Also power is analyzed using Xilinx Xpower analyzer.

In paper [6] it derives the accurate order of estimation formulae for the bandwidth extension filter, which is designed in mini max sense with the ripple constraints as the design criteria. The derived filter order estimation is significant in evaluating the computational complexity from the view point of the Top-level system design. A bandwidth extension method for ADCs and utilizing FIR filters designed in the Mini max sense was also proposed.

In paper [7] an algorithmic approach to the design Low power frequency selective digital filters based on in the concepts of adaptive filtering and approximate processing was elaborated. Adaptive filtering and approximation processing concepts are combined to design digital filters which have the important

property that the filter order can be dynamically varied in accordance with the stop band energy of the input signal.

In paper [8] a smoothing FIR filter is addressed for discrete time invariant state space polynomial models commonly used to model signals over finite data. An application is given for the time interval errors of local slave clocks of digital communication networks. In paper [9] to design the optimal finite wavelength FIR filter for the application of a general purpose integer programming using computer program. In paper [10] Distributed Arithmetic has been used to implement a bit serial scheme of a general asymmetric version of an FIR filter taking optimal advantage of 3 input LUT based structure of FPGA.

In paper [11] design and implementation of low pass, high pass and band pass fir filter using Spartan -6 FPGA device. The EDA tool is used to define filter order and coefficients, FIR filter is used for simulink simulation.

### V-RESULTS AND DISCUSSION

In this novel architecture the need for delay optimized system design of FIR filter architecture was discussed based on the various delay constrained architectures available which already exists. And different architectures of FIR filter for 4-tap, 8-tap, 12-tap can be implemented on the FPGA using Spartan 3E using

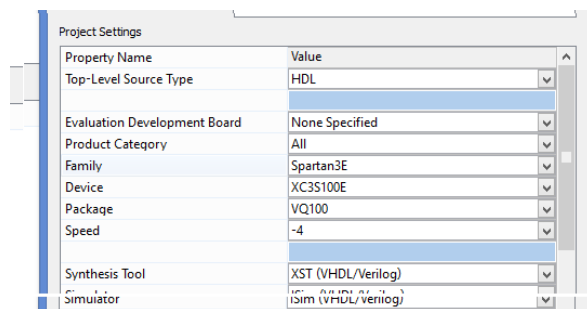


Fig.5 Target device

Verilog code for making a proposed technique which leads to the optimized delay in trade of with area and delay.

### Simulation output

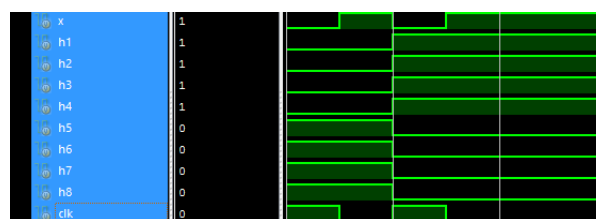
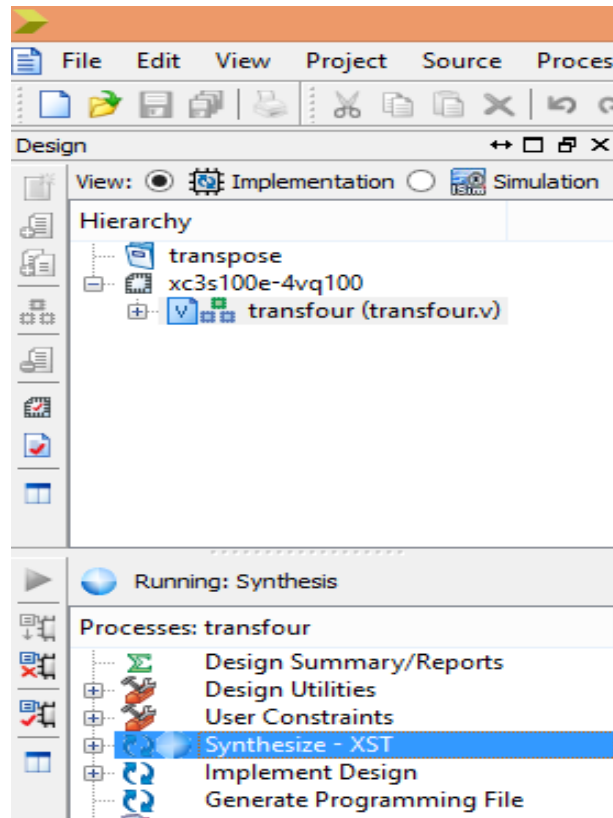


Fig.6 Simulation output

Plan for optimization of delay-power product in trade of with area is also suggested as bit serial and bit parallel implementation using pipelining and parallel processing can be done using the tool Xilinx system design to make a novel delay constrained FIR filter architecture.



**Fig. 7 Synthesis Report**



**Fig.8. FPGA kit used for Implementation**

**Table 1: Result Comparison Table**

Type of Architecture	No. of Slices	No. of LUTs	Delay in ns	Power in watts	Delay-Power Product
8-tap FIR Filter Transpose form	4	8	7.508	8.113	60.9124
8-tap FIR Filter	4	4	6.113	8.113	49.594

Direct form					
8-tap FIR Filter 1-level pipelined Direct form	4	7	7.412	8.113	60.133
8-tap FIR Filter 2-level pipelined Direct form	7	8	8.667	8.113	70.3
8-tap Lattice FIR Filter	5	10	8.39	8.113	68.06

By this analysis on survey of various literatures, it was concluded that the reduced power-delay product can be obtained for design of FIR lattice filter architecture with pipelining and parallel processing approach with optimum usage of number of adders and multipliers. Due to reduced delay this architecture will find applications in high speed system design like system on-chip and Network on chip. Also found applications in high speed system design in making decision in the medical field by analyzing various parameter which are related. These architectures are implemented using FPGA can be done as in the form of micro chip.

## REFERENCES

1. Rashmi Patil<sup>1</sup>, Dr.M.T.Kolte<sup>2</sup>, VLSI Implementation FIR Filter for Discrete Wavelet Transform, international Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering , Vol. 4, Issue 1, January 2015 .
2. Kai-Yuan Jheng, Shyh-Jye Jou\*, and An-Yeu Wu, a design flow for multiplier less linear-phase fir filters :from system specification to verilog code,2004.
3. Ms.Ritu Sharma, Prof. Ravi Mohan Verma, FPGA Implementation of Fast Fourier Transform (FFT) Based Finite Impulse Response(FIR)filterUsingVHDL, International Journal Of Engineering And Computer ScienceISSN:2319-7242Volume 3 Issue 3 March-2014.
4. Miss Pooja D Kocher, Mr. U A Patil, “Implementation and Comparison of Low Pass FIR Filter on FPGA Using Different Techniques”, International Journal of Innovative Research in Science, Engineering and Technology,Vol. 2, Issue 9, September 2013.
5. Bahram Rashidi, Farshad Mirzaei, Bahman Rashidi, and Majid Pourormazd, Low Power FPGA Implementation of Digital FIR Filter Based on Low Power Multiplexer Base Shift/Add Multiplier, International Journal of Computer Theory and Engineering, Vol. 5, No. 2, April 2013.
6. Yinan Wang, Hakan Johansson, Hui Xu, and Jietao Diao, Minimax Design and Order Estimation of FIRFilters for Extending the Bandwidth of ADCs, 4 Mar 2016.
7. Jeffrey T.ludwig , hamid nawab, Ananta p. chandrasekaran, low power digital filtering using approximate processing, ,IEEE journals of solid state circuits, NO:3 Volume 31,March 1996.
8. Ibarra-Manzano Oscar, Shmaliy Yuriy S., and Morales-Mendoza Luis, smoothing fir filtering of discrete state-space polynomial signal models, Conference Paper in Acoustics, Speech, and Signal Processing, 1988. ICASSP-88., 1988 International Conference on June 2011.

9. DUSAN M. KODEK, MEMBER, IEEE, Design of Optimal Finite word length FIR Digital Filters Using Integer Programming Techniques, IEEE transactions on acoustics, speech, and signal processing, vol. Assp-28,no. 3, June 1980.
10. P.Sravanthi,CH.Srinivasa Rao, S.Madhava Rao, A Novel Approach of Area-Efficient FIR Filter Design Using Distributed Arithmetic with Decomposed LUT, IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 7, Issue 2 (Jul. - Aug. 2013).
11. Emmanuel S. Kolawole, Warsame H. Ali, Penrose Cofie, John Fuller, C. Tolliver, Pamela Obiomon, Design and Implementation of Low-Pass,High-Pass and Band-Pass Finite Impulse Response (FIR) Filters Using FPGA, Circuits and Systems, 2015, 6, 30-48 Published Online February 2015 in SciRes.