

# 15-Level Inverter Topology of Reduced Switch Count with Power Loss Analysis

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## Abstract

Inverters convert DC to AC. A multi-level inverter surpasses the capabilities of a traditional inverter, having developed to accommodate voltage applications and finding widespread commercial use. While conventional inverters yield the output in the shape of a square, inverters with multilevel are employed to generate a waveform that closely approximates a sinusoidal one. In comparison to traditional inverters, the 15-level inverter exhibits advantages such as reduced THD, the power quality of output power is improved by using the DC link with higher voltages, and switching losses are reduced. Multilevel inverters achieve these benefits by utilizing a smaller number of switches and generate closer to sinusoidal output. This particular approach involves the use of ten switches to generate output of 15 levels, contributing to a simplified circuit design.

**Keywords:** Asymmetric Inverter, Sinusoidal Pulse Width Modulation, Carrier Frequency, Phase Opposition, Phase Disposition, THD.

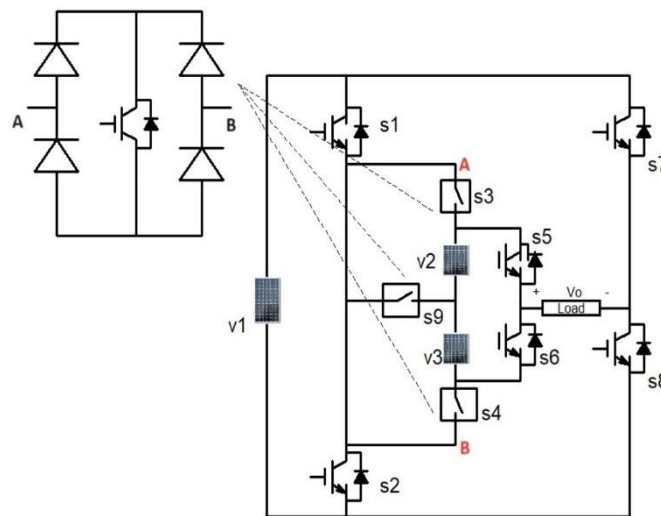
## I. INTRODUCTION

THE ADOPTION OF MULTI-LEVEL INVERTERS INCREASED CONSIDERABLE IMPORTANCE IN RECENT YEARS. VARIOUS COMBINATIONS OF POWER SEMICONDUCTOR SWITCHES ENABLE THE CREATION OF DIVERSE APPLICATIONS. AMONG THE VARIOUS CASCADED CONFIGURATIONS, THE CASCADED H-BRIDGE CONFIGURATION HAS GARNERED ATTENTION FOR ITS NOTABLE FEATURES, INCLUDING EASY CONTROL, OPERATIONAL FLEXIBILITY, AND A MODULAR STRUCTURE SUITABLE FOR VARIOUS MODULATION TECHNIQUES. IN RECENT TIMES, H-BRIDGE CONVENTIONAL INVERTERS HAVE BEEN EMPLOYED IN INDUSTRIAL APPLICATIONS DUE TO THEIR STRAIGHTFORWARD SWITCH CONFIGURATION AND SIMPLIFIED CONTROL MECHANISMS. HOWEVER, FOR CERTAIN APPLICATIONS, THEIR PERFORMANCE IS DEEMED UNSATISFACTORY DUE TO THE POOR QUALITY OF OUTPUT CHARACTERIZED BY EXCESSIVE HARMONIC COMPONENTS. TO ADDRESS THESE ISSUES, MULTI-LEVEL INVERTER TECHNIQUES ARE BEING ADOPTED IN INDUSTRIAL APPLICATIONS TO ALLEVIATE THE VOLTAGE LOAD ON POWER COMPONENTS AND GENERATION OF HIGH-CALIBER OUTPUT VOLTAGE. THE USE OF MULTI-LEVEL INVERTERS HAS EXPANDED ACROSS DIVERSE APPLICATIONS LIKE RENEWABLE ENERGY TRANSFORMATION, INDUSTRIAL PROPULSION, AND VARIOUS OTHER APPLICATIONS. EACH EXISTING INVERTER TOPOLOGY COMES WITH ITS LIMITATIONS. HENCE, THE TASK IS TO REDUCE WAVEFORM DISTORTIONS EFFECTIVELY BY SELECTING AN OPTIMAL SWITCHING FREQUENCY, ENSURING SUPERIOR POWER QUALITY AND MINIMAL OUTPUT DISTORTION.

**II. ARRANGEMENT OF THE SUGGESTED SYSTEM**

The topology illustrated in Figure 1 comprises eight unidirectional switches labeled  $S_1$  to  $S_8$ , in addition to a bidirectional switch,  $S_9$ . Among these switches, three, four and nine are bi-directional switches that integrates an IGBT switch with 3 diodes to facilitate bidirectional current flow. The three DC voltage sources share identical values. This paper explores the operation of the inverter through various Pulse Width Modulation. In pulse width modulation, the comparison between the main and carrier signals is a fundamental aspect. Assuming "N" as the required number of levels to generate, (N-1) carrier signals are needed for comparison with the sinusoidal signal, in this specific scenario, fourteen carrier signals are employed. Triangular signals are used as carriers. To compare with the reference signal, the peak magnitudes of the triangle carrier signals are distributed in a repeating sequence by dividing the reference signal into N equal parts.

The comparison results in the generation of fifteen distinct voltage level signals. The signals, namely  $V_1, V_2, V_3, V_4, V_5, V_6, V_7, V_8, V_9, V_{10}, V_{11}, V_{12}, V_{13}, V_{14}$  and  $V_{15}$  are assigned using GOTO variables. These voltage level signals are then directed to the OR gate. Switching GOTO variables ( $S_1$  to  $S_{10}$ ) represent the various modes of operation and are connected to IGBTs using FROM variables. These FROM variables facilitate the connection of all switching variables to the IGBTs, thus governing the overall switching behavior of the inverter. The implementation of logic gates and relational operators in MATLAB ensures the precise control and coordination of the switching variables, contributing to the effective operation of the cascaded H-bridge inverter.



**Figure 1: Fig. illustrating a 15-level inverter with reduced switches.**

The scope displays the voltage and current output waveforms across the load terminals, with an input of 50V, 100V, 150V for each DC voltage source.

**III. OPERATION AND MODULATION METHODOLOGY**

Since the voltage of all source voltages is non-uniform, let's designate the DC voltage sources as ' $V_{dc}$ ' and ' $3V_{dc}$ ' the illustrations depict various circuit voltage configurations achieved by adjusting gate pulses in accordance with voltage needs. The table below outlines the conditions under which switches become active for their corresponding voltage levels.

### Operating Modes:

The functioning of the 15-level inverter is elucidated with various generation modes as outlined below. In each operational mode, the active switches are illustrated in Figure 2. Switching combinations necessary for producing output of fifteen level voltages are detailed in TABLE-I. The fifteen modes of operation are as follows:

In the Level 1: Switches 1, 3, 5 and 7 are in ON state. The current flow path is illustrated in Figure 2(a).

In the Level 2: Switches 1, 3, 5 and 8 are in ON state. The current flow path is illustrated in Figure 2(b).

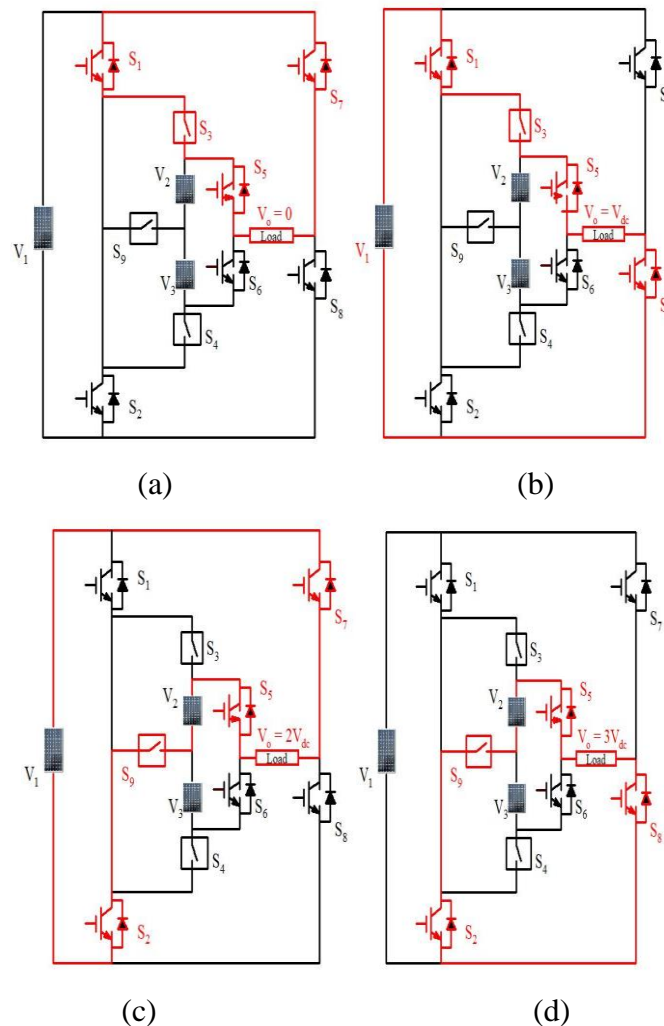
In the Level 3: Switches 2, 5, 7 and 9 are in ON state. The current flow path is illustrated in Figure 2(c).

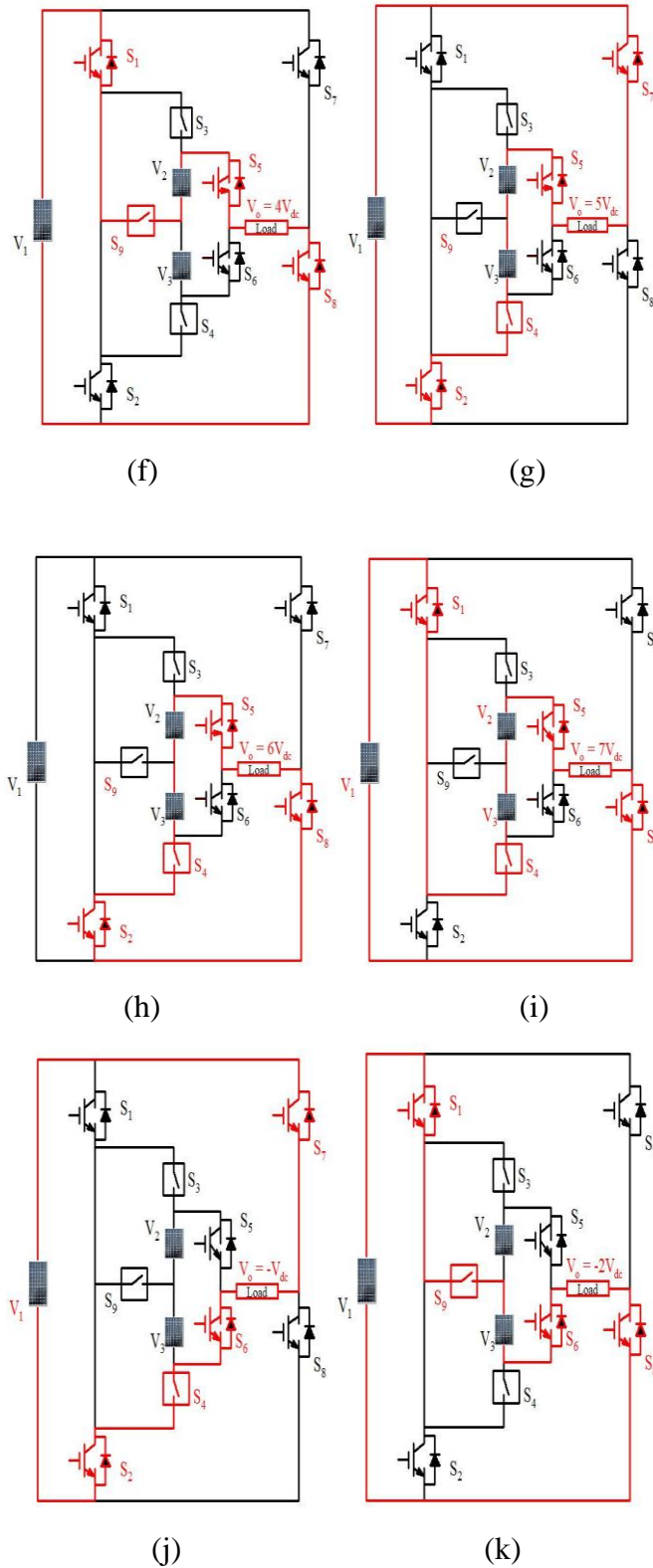
In the Level 4: Switches 2, 5, 8 and 9 are in ON state. The current flow path is illustrated in Figure 2(d).

In the Level 5: Switches 1, 5, 8 and 9 are in ON state. The current flow path is illustrated in Figure 2(e).

In the Level 6: Switches 2, 4, 5 and 7 are in ON state. The current flow path is illustrated in Figure 2(f).

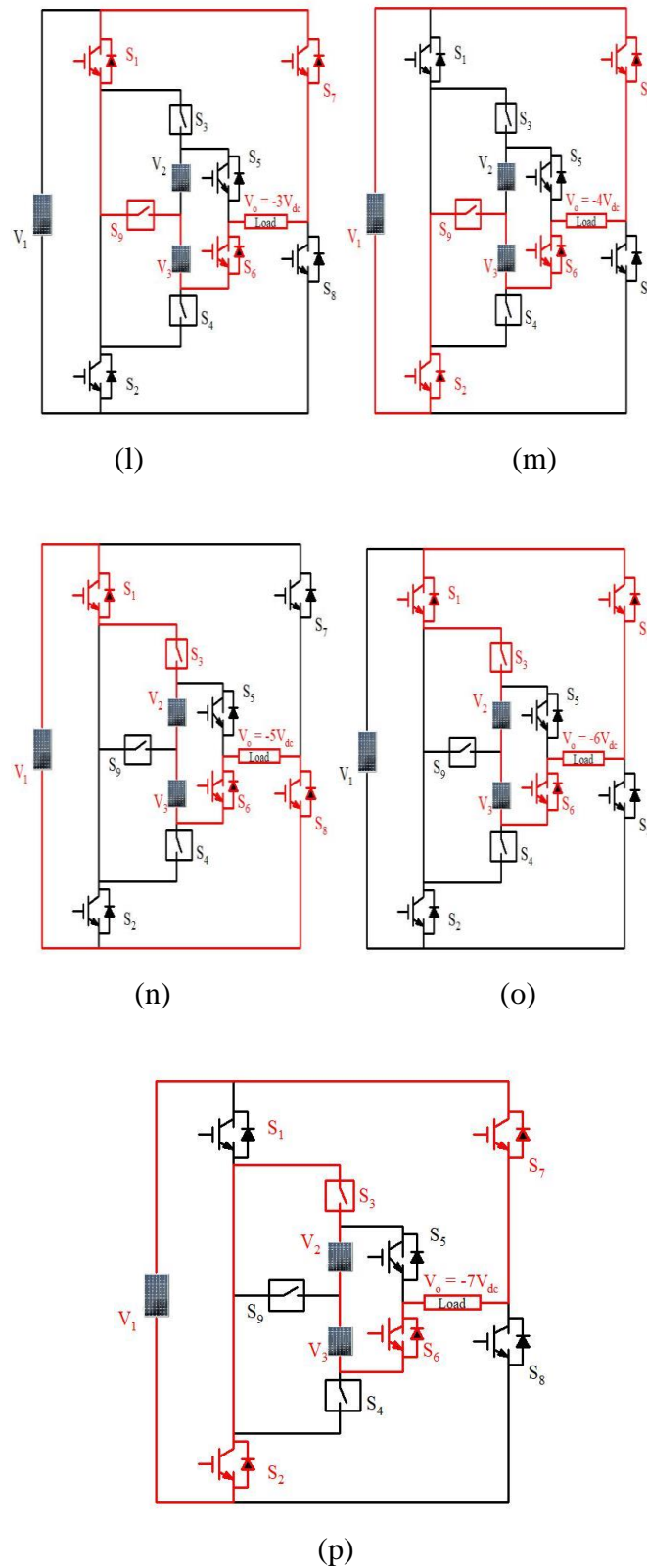
In the Level 7: Switches 2, 4, 5 and 8 are in the ON state. The current flow path is illustrated in Figure 2(g).





*In the Level 8:* Switches 1, 4, 5 and 8 are in the ON state. The current flow path is illustrated in Figure 2(i).

*In the Level 9:* Switches 2, 4, 6 and 7 are in the ON state. The current flow path is illustrated in Figure 2(j).



**Figure 2:** depicts the operational modes of the nine-level voltage produced by the proposed inverter.

*In the Level 10:* Switches 1, 6, 8 and 9 are in the ON state. The current flow path is illustrated in Figure 2(k).

*In the Level 11:* Switches 1, 6, 7 and 9 are in the ON state. The current flow path is illustrated in Figure 2(l).

*In the Level 12:* Switches 2, 6, 7 and 9 are in the ON state. The current flow path is illustrated in Figure 2(m).

*In the Level 13:* Switches 1, 3, 6 and 8 are in the ON state. The current flow path is illustrated in Figure 2(n).

*In the Level 14:* Switches 1, 3, 6 and 7 are in the ON state. The current flow path is illustrated in Figure 2(o).

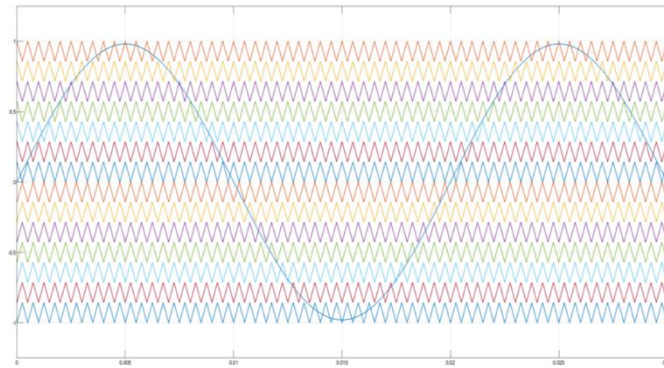
*In the Level 15:* Switches 2, 3, 6 and 7 are in the ON state. The current flow path is illustrated in Figure 2(p).

Levels	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>	S <sub>7</sub>	S <sub>8</sub>	S <sub>9</sub>
7-Vdc	1	0	0	1	1	0	0	1	0
6-Vdc	0	1	0	1	1	0	0	1	0
5-Vdc	0	1	0	1	1	0	1	0	0
4-Vdc	1	0	0	0	1	0	0	1	1
3-Vdc	0	1	0	0	1	0	0	1	1
2-Vdc	0	1	0	0	1	0	1	0	1
1-Vdc	1	0	1	0	1	0	0	1	0
0	1	0	1	0	1	0	1	0	0
-1-Vdc	0	1	0	1	0	1	1	0	0
-2-Vdc	1	0	0	0	0	1	0	1	1
-3-Vdc	1	0	0	0	0	1	1	0	1
-4-Vdc	0	1	0	0	0	1	1	0	1
-5-Vdc	1	0	1	0	0	1	0	1	0
-6-Vdc	1	0	1	0	0	1	1	0	0

-7-Vdc	0	1	1	0	0	1	1	0	0
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**TABLE 1:** illustrates the switching operations corresponding to the nine-level output voltage.

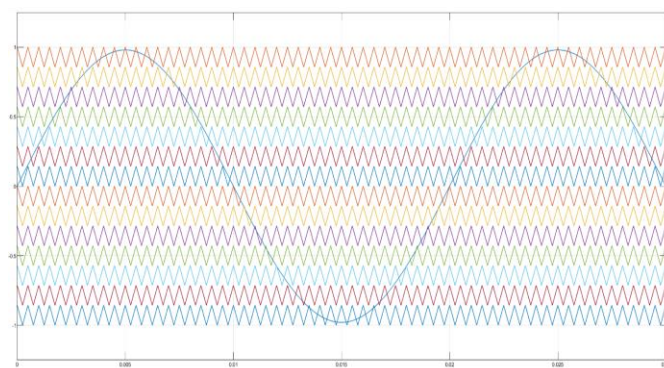
**A. Modulation Method-POD PWM:**



**Figure 3: Phase Opposition Disposition PWM Technique**

In an N-level inverter employing Phase-Shifted (POD SPWM) technique with (N-1) carrier waves, a specific scenario arises when the carrier waves above and below the zero reference are synchronized, while the carrier wave below the reference is a mirror image of the carrier wave above the reference. This configuration leads to improved harmonic levels, particularly at lower modulation indices. Furthermore, the figure 3 shows the replication process is conducted at a fundamental frequency of 50 Hz and a carrier frequency of 2 kHz, contributing to enhanced performance. The voltages of values 50V, 100V, 150V are considered as input voltages for each dc source. The scope displays the waveforms of voltage and current outputs across the load resistor.

**B. Modulation Method-PD PWM:**

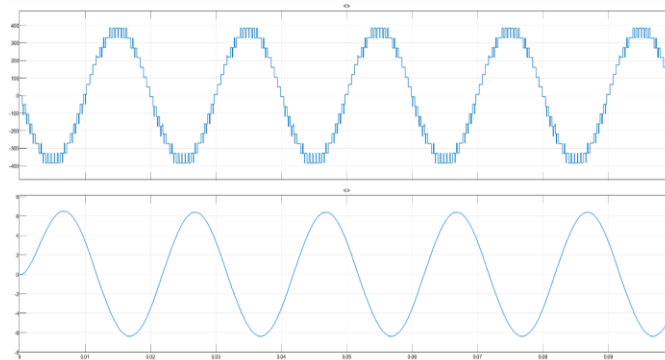


**Figure 4: Phase Disposition Pulse Width Modulation Technique**

Switching pulses required for the 15-level multilevel inverter working using PD-PWM technique are employed. In Figure 4, the switching pulse is illustrated, and it examines every tier of the carrier triangle waveform in comparison to the sinusoidal signal waveform as reference. The pulses are created and administered to the inverter switches whenever the value of the modulating signal exceeds of the reference signal at all levels.

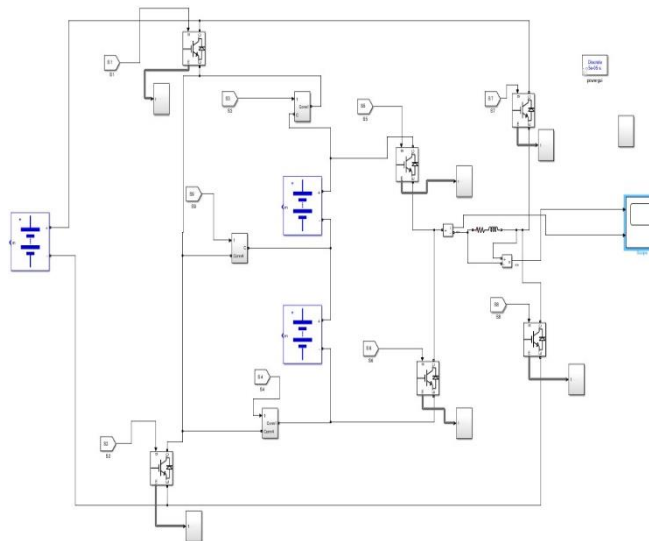
#### 4. RESULTS AND ANALYSIS

Ultimately, the voltage of DC input is transformed into fifteen-level increments resembling a sinusoidal pattern of varying voltage magnitudes over time. Figure 5 displays the output voltage characterized by fifteen distinct levels. Assessing the efficiency of the inverter necessitates the determination of total power losses. The paper validates the analysis of power losses for this purpose.



*Figure 5: Proposed 15-level inverter Load Current and Voltage waveforms for an R-L load.*

#### 5. SIMULATION



*Figure 6: A schematic depicting the Modified Cascaded H-Bridge Inverter Simulation circuit.*

Figure 6 depicts the schematic diagram of the Modified Cascaded H-Bridge multilevel inverter. Firing pulses are routed to the IGBTs via 'FROM' variables, which transmit active signals obtained from the 'GOTO' variables of S1, S2, S3, S4, S5, S6, S7, S8, S9, and S10. The generation of firing signals depends on the selected PWM technique, and this PWM function is performed within the subsystem.

Each switch is equipped with a measurement port, offering average current, average voltage, RMS current, and RMS voltage values via the display. These values play a crucial role in computing power losses. The examination encompasses three pulse width modulation techniques—PD-PWM, PO-PWM, and APOD-PWM—all conducted at a frequency of 2KHz.



## 6. ANALYSIS OF POWER LOSS IN INVERTERS

Power electronic switching devices are classified into three types of losses: conduction losses, switching losses, and blocking or leakage losses. Leakage losses are often ignored. In modeling and analysis, IGBTs act as power electronic switches. The type of switch used has an impact on power loss analysis since various switches require different operational procedures. Switches and diodes linked in anti-parallel to a switching device experience conduction loss. However, this analysis does not account for losses generated by anti-parallel diodes, as well as conduction losses from switches. The word 'P<sub>ci</sub>' refers to conduction losses in switches. The following equation shows the conduction losses experienced by switches.

$$P_{ci} = \mu_{CE0} * I_{avg} + r_c * I_{rms}^2 \text{ -----(1)}$$

Where,

$\mu_{CE0}$ : Voltage across the collector-emitter terminals when the collector current is zero.

$I_{avg}$ : Mean current flowing through the switch.

$r_c$ : collector-emitter on-state resistance

$I_{rms}^2$ : root mean square (rms) current through the switch

The values for ' $\mu_{CE0}$ ' and ' $r_c$ ' which are specified as 0.0054V and 0.8 ohms, ' $I_{avg}$ ', ' $I_{rms}$ ' of each switches are determined via inverter simulation.

Switching losses are another kind of loss. Switches and diodes connected in anti-parallel to a switch experience switching losses. However, this study ignores switching losses in the reverse-biased diode and instead focuses entirely on switching losses within the switches. The equation below depicts the switching losses caused by switches.

$$P_{sw} = (E_{on} + E_{off}) f_{sw} \text{ -----(2)}$$

Where,

$E_{on}$ : Energy dissipation during IGBT conduction

$E_{off}$ : Energy losses during IGBT non-conduction

$f_{sw}$ : Switching frequency of IGBT

Fixed values " $E_{on}$ " and " $E_{off}$ " are obtained from the IGBT MGW12N120D datasheet and are specified as 0.55 watts each. The switches are operate with the frequency denoted by " $f_{sw}$ ," which corresponds to the carrier signal frequency, as switches are synchronize with it. Modulation frequency could be computed from values in repetitive elements. Conduction and switching losses are determined from equations (1) and (2).

$$PD = PD_{cond} + PD_{switch}$$

$$PD_{cond} = I_{rms}^2 * R_d + V_F * I_{avg}$$

Where,

$V_F$ : Threshold voltage

$R_d$ : Dynamic resistance

The switching losses can be represented as:

$$PD_{switch} = 1/2 C_R * V_R^2 * f_{sw} + 1/6 I_{RR} * V_R * t_b * f_{sw}$$

### 7. OBSERVATIONS

The experimental data for the Modified 15-level Cascaded H-Bridge Multilevel inverter were obtained under specific conditions: an input DC voltage of 150V, 100V, and 50V for each level, a load resistance of 80 ohms, and a carrier frequency of 2KHz using the Phase Opposition Disposition pulse width modulation technique.

Switches	Diodes	I <sub>rms</sub> (A)	I <sub>avg</sub> (A)
	D1	2.801	1.517
S3	D2	0.7849	0.1706
	D3	0.7849	0.1706
	D4	1.517	2.801
	D1	1.492	0.4677
S4	D2	1.532	0.4924
	D3	1.532	0.4924
	D4	1.492	0.4677
	D1	1.424	2.735
S9	D2	0.09395	0.5952
	D3	0.09395	0.5952
	D4	1.424	2.735

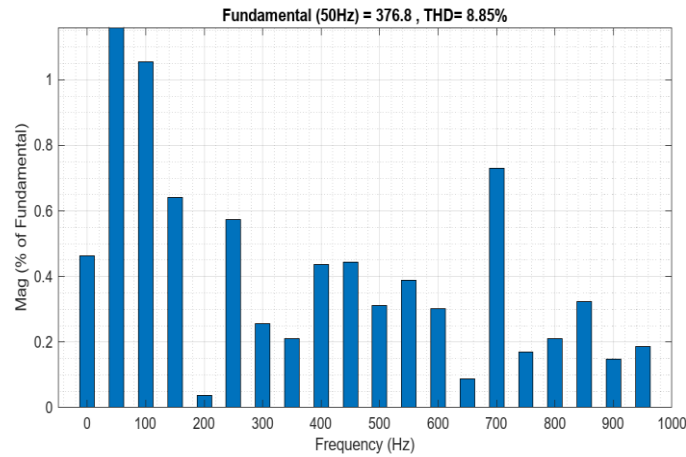
S.No	Switches	V <sub>rms</sub> (V)	I <sub>rms</sub> (A)	P <sub>ci</sub> (W)
1.	S1	38.77	3.293	8.6734
2.	S2	40.76	3.172	8.0479
3.	S5	233.4	3.261	8.5166
4.	S6	241.8	3.209	8.2476
5.	S7	38.46	3.3	8.7176
6.	S8	41.05	3.166	8.0243

**TABLE II: Observations of switches 15-Level inverter with POD-PWM technique.**

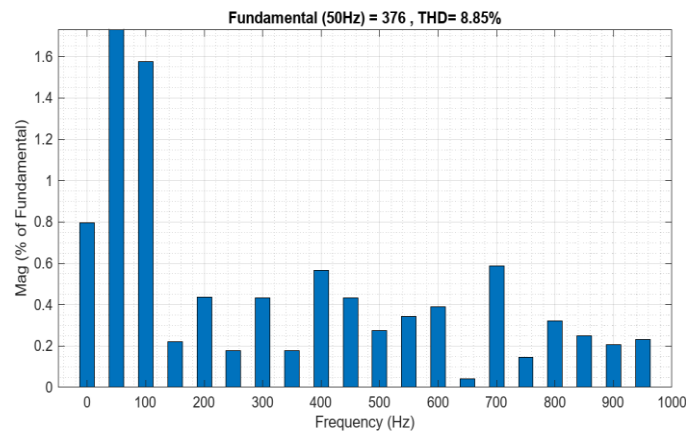
Parameters	Values
Output R.M.S Voltage	268.7V
Output R.M.S Current	4.3A
Output Power	1143.8W
Efficiency	97%

**TABLE III: Results from the simulation of 15-Level inverter.**

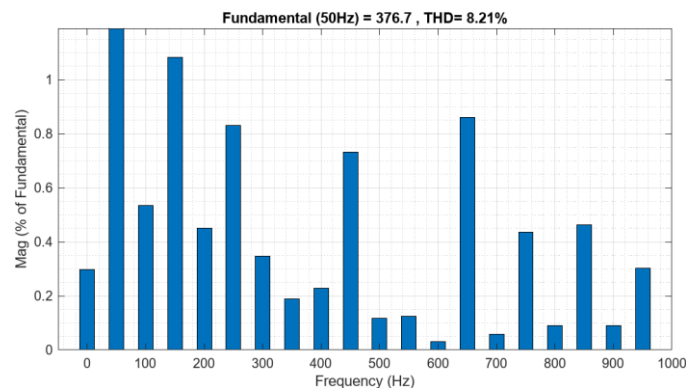
**A. Voltage THD levels at the carrier frequency of 2KHz**



*Figure 7: THD levels of the inverter, with PD-PWM technique with the carrier frequency of 2KHz.*



*Figure 8: THD levels of the inverter, with PO-PWM technique with the carrier frequency of 2KHz.*



*Figure 9: THD levels of the inverter, with POD-PWM technique with the carrier frequency of 2KHz.*

*B. Percentage values indicating voltage Total Harmonic THD levels of 15-level inverter by using different PWM techniques.*

S.NO	Name of the inverter	PWM Technique	Carrier frequency	Voltage THD Level
1.	15-Level inverter	PD	2KHz	8.85
2.	15-Level inverter	PO	2KHz	8.85
3.	15-Level inverter	POD	2KHz	8.21

## 8. CONCLUSION

A revised cascaded H-bridge inverter employing three distinct PWM techniques achieves fifteen voltage levels, yielding minimal Total Harmonic Distortion (THD) levels and improved efficiency. This configuration decreases the quantity of switches in contrast to traditional inverters., resulting in cost and weight reduction. Among the PWM techniques, Pulse Overlap Duty (POD)-PWM proves most favorable with regard to THD levels. Notably, the POD-cascaded H-bridge inverter operating at a 2KHz carrier frequency demonstrates the lowest voltage THD percentage at 8.21%, alongside a high efficiency rating of 97%.

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