

# An Efficient Multi-Level Vending Machine FSM Using Kintex-7 FPGA

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## ABSTRACT

The need for efficient multi-level product vending machines is in high demand. In this paper, we propose a multi-level effective vending machine design using a finite state machine (FSM), with the targeted FPGA being Kintex-7. The proposed design was developed in Verilog HDL to achieve better performance in terms of speed, power and area. The proposed design efficiency is validated using XILINX ISE 13.2.

**Keywords:** FSM-Finite State Machine, FPGA- Field Programmable gate array, HDL-Hardware Description Language.

## 1. INTRODUCTION

The vending machine is automated. The electronic machine is used in the biggest shopping malls. It gives outputs such as snacks, beverages, and lottery tickets after consuming money from consumers.

This proposed vending machine is modelled to serve ₹ 5 and ₹ 10-based products according to user choices. This design supports user choices using selective inputs and performs effective transactions [1] and [2] with high speed.

## 2. PROPOSED VENDING MACHINE

The proposed design is developed based on the following flow chart Fig-1. This design takes input from the user in terms of coins and offers the available products. If the user opts for the products available among the served products using the select option, it will serve the products. If the user has not selected it, it will be waiting for further inputs from the user. The machine provides the option for the user to go to the next level of products served [4] [5]. In this case, the user has to add sufficient currency to get to know the products served at the next level. If the user opts for the next level of products by selecting the product, then the machine will deliver the selected product. If not, after the waiting period, the user amount will be returned. This machine serves the products based on the user's choices effectively, or else the transactions will be executed perfectly.

## 3. PROPOSED FINITE STATE MACHINE

The following Fig 2 is the FSM developed for intended Vending machine.

**S0:** Initial state: No products available.

**S1:** Level-1 products- are available at ₹ 5.

**S2:** Level-2 products- are available at ₹ 10.

**S3:** Level-3 products- are available at ₹ 15.

**S4:** Level-4 products- are available at ₹ 20.

**S:** selection line: if S = 1, the product is served; if S = 0, If S=0 it is in a waiting state.

When the machine is in the S0 state, if the user inserts a coin based on the input, it goes to the next state and offers the available products in the respective state. If the user selects the product using 'S', it will serve the product, or else it is in a waiting state for further inputs in terms of coins. [3] [4] If the user adds the currency, it goes to the next state as per the inserted currency value and offers the products; if the user selects the product, it will deliver; otherwise, after a waiting period, the amount will be returned.

#### 4. HDL IMPLEMENTATION

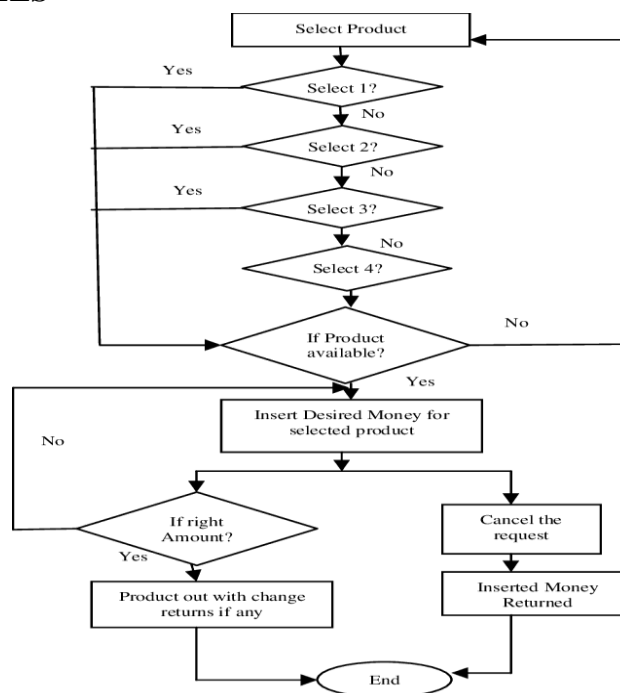
This FSM has been implemented using Verilog HDL in the XILINX ISE 13.2 environment on the Targeted FPGA Board Kintex-7.

The above figures Fig-3 and Fig-4 shows the is the RTL, technological Schematic of Proposed vending machine on the targeted FPGA KINTEX-7 with 7 LUT-FF pairs and 22 Slice LUT.

#### 5. RESULTS DISCUSSION

This proposed design is simulated and synthesized using the KINTEX-7 FPGA on the XILINX ISE 13.2 environment is shown in the Fig-5. The state transition is based on the user input at the positive edge trigger of CLK. In the above fig-4, we can verify the output is high at the second positive edge triggering of the clock. The below fig-6. shows the synthesis report of the proposed vending machine. The proposed vending machine consumes 0.107 W of low power and high-speed performance with a delay of 0.515 ns.

#### 6. FIGURES AND TABLES



**Fig 1: Flow chart of the vending machine.**

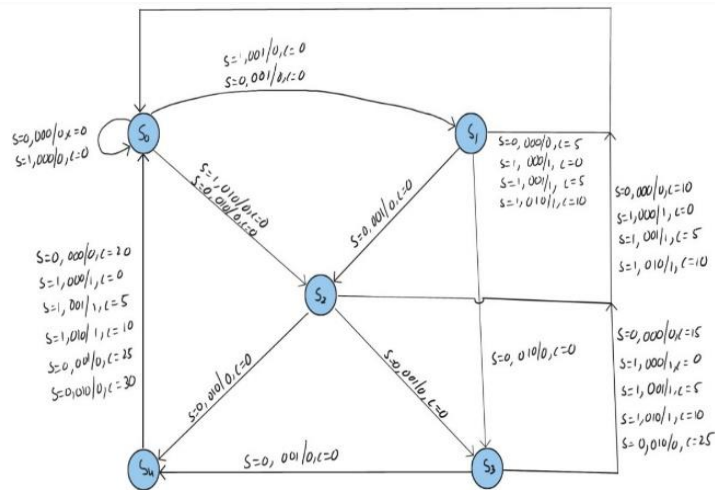


Fig 2: State diagram of the Proposed vending machine.

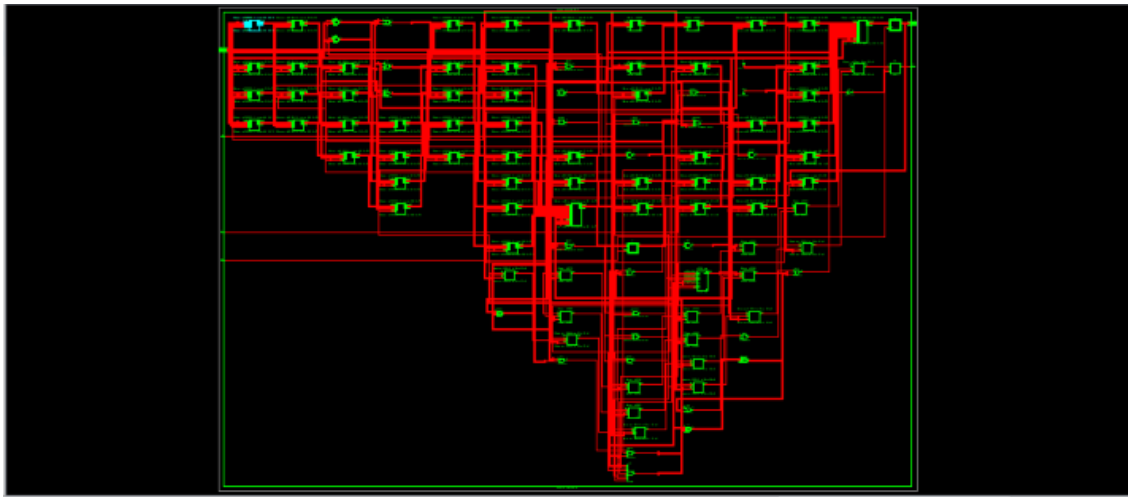


Fig 3: RTL Schematic of Proposed vending machine.

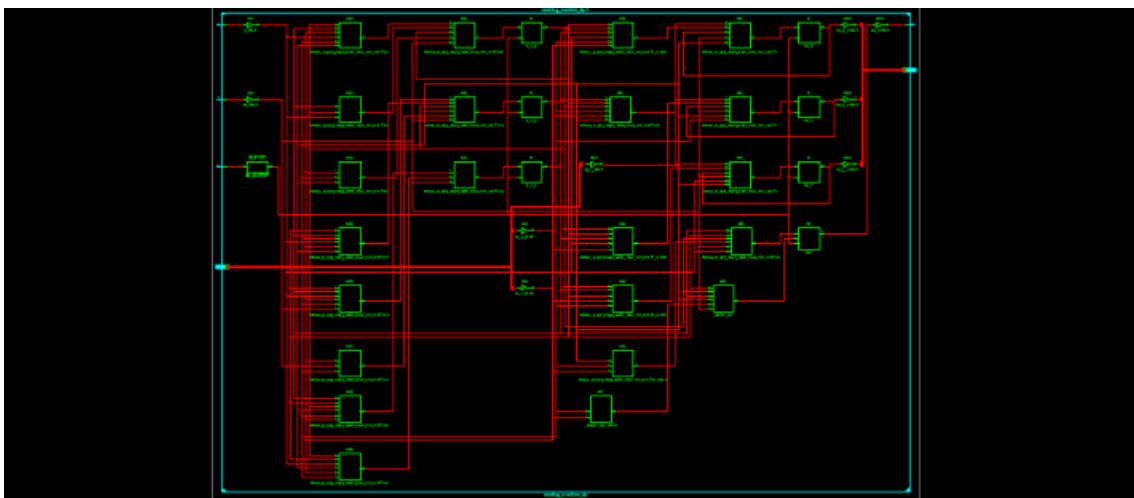
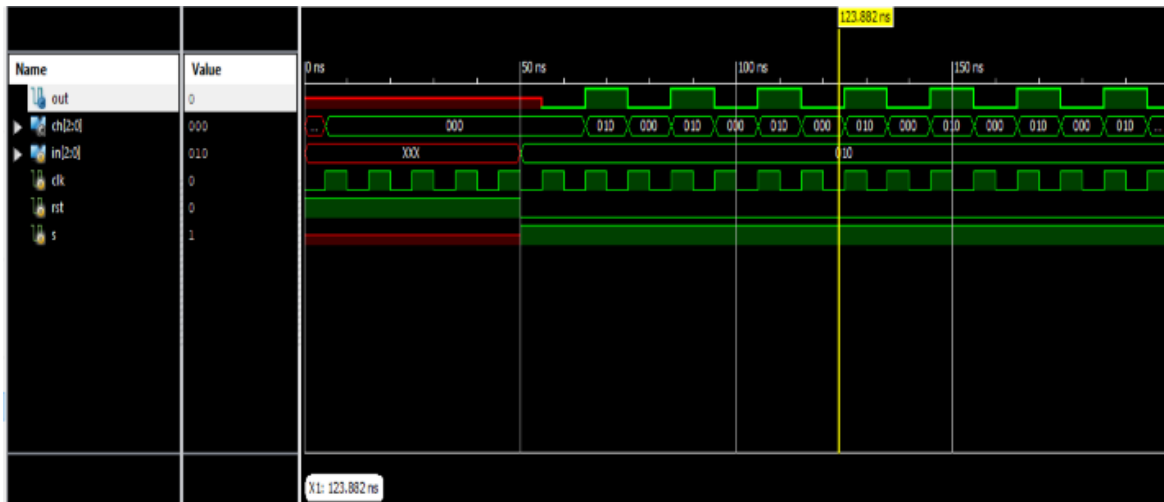


Fig 4: Technological schematic of the Proposed vending machine.



**Fig 5: Simulation Waveform of the Proposed Vending Machine.**

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Data Path: ch_2 to ch<2>
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Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FD:C->Q	2	0.232	0.283	ch_2 (ch_2)
OBUF:I->O		0.000		ch_2_OBUF (ch<2>)
<b>Total</b>		<b>0.515ns (0.232ns logic, 0.283ns route)</b> (45.0% logic, 55.0% route)		

**Fig 6: Delay obtained by Proposed Vending machine.**

FPGAs	Delay Offered (ns)
<b>Virtex-7 Low Voltage</b>	<b>0.701</b>
<b>Artix-7</b>	<b>0.645</b>
<b>Kintex-7</b>	<b>0.515</b>
<b>Kintex-7 Low Voltage</b>	<b>0.701</b>

**Fig 7: Comparison of Kintex-7 with Different FPGAs**

## 7. CONCLUSION

The proposed design supports multi-level products with high speed and low power consumption. The proposed model using the KINTEX-7 FPGA offers better performance compared with other FPGAs. This architecture offers a 0.515 ns delay and 0.107 W of low power shown in the Fig-7.

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