International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

# Challenges for Leading Edge Node FINFET

**Selva Lakshman Murali**

Silicon Design Engineer, Arizona State University

**Abstract:**
The primary focus of this work is to find out the challenges associated with 7nm node finFET. To enable the current generation of gadgets/instruments, foundries are going toward smaller geometries (FinFET 7nm, 5nm, etc.) for manufacturing SOC/ASIC. To support the 7nm technology node without EUV, the Layout Design Rules have been scaled quite aggressively. As a result, obtaining satisfactory performance and yield in High Volume Manufacturing (HVM) has become a difficult undertaking. The gains in terms of power, performance, and other characteristics that become available with reduced geometries are the main drivers driving this movement. Analog/mixed-signal circuits, on the other hand, do not fully achieve these gains. They get increasingly difficult to design, with higher parasitic resistance and capacitance, more layout-dependent effects, and, in certain cases, layout growth. While in terms of fabrication the challenges are in node and cost, mask making, patterning, transistor formation, BEOL, MEOL, Technology parasitic elements and process control etc. This indicate what are the challenges for design of 7nm node FinFET.

## INTRODUCTION

The semiconductor business is seeing a larger spectrum of technical breakthroughs as demand for semiconductor products/services grows in tandem with the exponential growth in customer expectations. Starting at the 16/14nm nodes, FINFET technology is currently available on cutting- edge electronics devices. A 7nm finFET will be an evolutionary step forward from 16nm/14nm and 10nm finFETs. As the industry moves toward 7nm, the use of more sophisticated multiple patterning techniques for the FIN, Gate, different Middle Of Line (MOL)architectures, and Back End Of Line (BEOL) wiring levels will put significant pressure on density to offset the extra cost. At 7nm, chipmakers are uncertain to make any significant structural or material modifications. At 7nm, however, one technology stands out above the rest: lithography. Originally, foundries planned to use extreme ultraviolet (EUV) lithography for this node. However, EUV will not be ready for the early phases of 7nm as it stands now, forcing the industry to rely on traditional 193nm immersion and multiple patterning. Patterning will bring the most challenges and innovations.

We're going to push the lithographic rules to their breaking point. Multi-Work function solutions for identical gate polarity will be driven by the need to reduce doping in FINFETs. Similarly, the requirement for improved transistor performance will lead to the development of new channel materials. To lower parasitic capacitance and resistance at the MOL and BEOL levels, new materials will be required. Certain variants of the 10nm node will be referred to as "7nm," just as some variants of the 20nm node were referred to as "16/14," but real "7nm" node circuit densities will necessitate the next generation of lithography, EUV at 13.5nm wavelength. The cost of the chip, which is challenged by the requirement for unique cost-intensive patterning techniques, is the key to acceptance in the electronics device area. Given the higher wiring parasitic, the ability to gain more performance at constant chip

power will be the key to adoption in the server area. To get to mature 7nm nodes, new materials will be required in all scenarios. And if that isn't enough, there are more difficulties at 7nm. In addition to the issues that come with repeated patterning, such as edge placement inaccuracy, pitch wandering, and expense, connection RC latency is a significant constraint in performance scaling. Customers at foundries are starting to grasp the design problems with 7nm. They'll also need to figure out how to deal with production challenges in order to set more realistic design deadlines. Semiconductor Engineering has looked at some of the more difficult process processes at 7nm to help the industry move ahead of the manufacturing curve. Masking, patterning, transistor creation, interconnects, and process control are all included.

## FABRICTION CHALLENGES

### A. Mask Making

First Chipmakers plan to use two types of lithography processes, EUV and immersion/multi-patterning, in tandem at 7nm. However, the state of EUV at 7nm is yet unknown. Chipmakers intend to adopt 193nm immersion/multi- patterning at first. After that, if it's ready, EUV will be added to some layers later. EUV will drop to 5nm if it isn't ready. Lithography, like before, defines the photomask type and specifications. The photomask is an important component of the flow. The mask is finished and transported to the fab. A lithography tool is used to lay the mask. The tool then shines light through the mask, causing the images on the wafer to be patterned. At each node, making a mask becomes more complicated. At 40nm half-pitch, for example, 193nm wavelength lithography reached its physical limit. EUV allows for significant reductions in the complexity of 7nm patterning technology. Given the aforementioned parameters, it is evident that EUV will be used in the MOL and lower BEOL levels, where multiple 3 and 4 pass patterning levels can be reduced to a single EUV exposure level. This will improve wiring capability and allow for circuit-level scaling to be improved.

Photomask makers must utilize several reticle enhancement methods (RETs) on the mask to deal with diffraction concerns at advanced nodes. Optical proximity correction (OPC) is one RET that is used to change mask patterns in order to improve wafer printability. At each node, OPC takes use of aid characteristics, which are becoming smaller and more complicated. At each node, the number of masks per mask set is also rising. According to a survey conducted by the eBeam Initiative, there are 60 masks per mask set at 16nm. According to the poll, at less than 11nm, this figure is predicted to rise to 77. Multiple patterning increases the total number of masks required to make a chip. This already puts a strain on the time it takes to make each mask, but the patterns themselves are becoming increasingly intricate. This is due to the fact that each feature must be written more accurately. "To acquire the requisite process window, more aggressive OPC, such as ILT (inverse lithography techniques) or forms approaching ILT shapes, is required." "This complicates mask designs and necessitates finer geometries and spacing for the mask." As a result, writing or patterning the mask with today's e-beam mask writers will take longer. As a result, clients will see longer mask turnaround times and increased expenses. "Additionally, rising mask complexity and the need for geometries smaller than 60nm necessitate model-based processing," says the author. "Traditional fracturing isn't enough." We believe that GPU acceleration's computational advantage allows for accurate model-based processing on the 7nm node." Meanwhile, mask producers will have to deal with the complexity of EUV masks if the industry inserts EUV at 7nm. Sub resolution assist features (SRAF) on the mask for EUV range from 32nm to 40nm, whereas optical SRAFs are 60nm. According to Mentor Graphics, the SRAF 1x design sizes for EUV

range from 8nm to 10nm, compared to 15nm for optical. Overall, EUV masks take a long time to write. Photomask manufacturers want a new type of multi- beam mask writers to reduce write times. However, it remains to be seen whether these tools will be ready in time for 7nm.

For printing contacts and the lowest metal levels, pitch splitting or litho-etch-litho-etch (LELE) debuted at 20 nm (Fig. 1(a)). The remaining unprinted alternate lines are exposed with a second resist pattern after a pattern of alternate lines (Mask A) is transferred to a thin hard mask (Mask B). The combined hard mask and resist patterns are then transferred to the underlying layer using a standard etch. Pitch splitting complicates layout coloring or mask decomposition by introducing new criteria for dealing with misalignment tolerance and pattern density balance between the two masks. A third mask (LELELE) can be added to this approach to further lower metal pitch to 48 nm.

To shorten line end-to-end spacing, cut masks are utilized (Fig. 1(b)). Cut patterns slice through a pattern of continuous lines without line end corner rounding or pullback artifacts in an orthogonal direction. The chopped ends' artifacts aren't transferred to the final pattern because they're outside the line patterns. Depending on whether the line pattern is positive tone (e.g., gate) or negative tone (e.g., gate), the cuts can be used as an extra exposure or a hard mask pattern (e.g., metal trench). Cut masks were first used in 45-nm gate patterning for denser SRAM cells, and they've since become commonplace in fin, gate, and interconnect patterning. Pitch- splitting the cuts has become necessary in 10 nm and below due to the tight cut pitch.

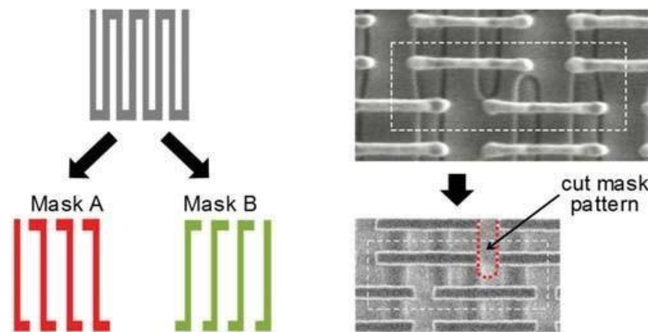



**Fig. 1. (a) Pitch splitting and (b) use of cut mask.**

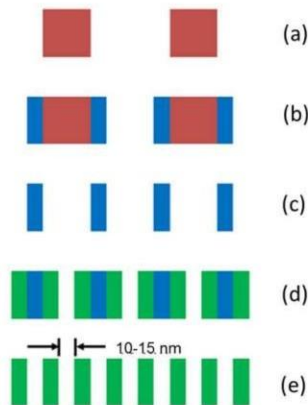
## B. Patterning

At advanced FINFET nodes, the limits of traditional 193nm immersion lithography have produced a range of patterning approaches. The FIN level will be patterned by SAQP techniques pioneered by the semiconductor memory industry at advanced 10nm and 7nm nodes, for example. This method entails first creating a mandrel and then adding spacers to double the patterning frequency. After that, these spacers are employed as mandrels to quadruple the lithographically printed pitch. This can be seen in Figure 2 below. This approach has resulted in a number of hard mask materials, which are utilized to transfer the final design to a hard mask, which is then used to pattern the FIN in a single etch. While this is a clever solution (the resist strips are applied to the hard mask, shielding the underlying FIN material), it does not address the imperfections of three non- lithographic voids between the final FINs. Because the connections to the transistors are made at the ends of the FINs by creating an epitaxial (Epi) layer for the transistor's source and drain, this is a key issue. The volume of this Epi layer is proportional to the distance between the FINs, and it has traditionally been employed to strain the FINs and lower the FIN contact resistance. As a result, SAQP patterning of the FINs introduces new diversity into the device's performance and resistance.

Because the gate pitch will be more than 40nm, the gate level is patterned using Self-Aligned Double

Patterning (SADP). At 14nm, SADP for the FIN level is widely used, and the industry has figured out how to limit variability. The necessity to print gates of different length for input-output (I/O) devices with greater dielectric thickness and the use of longer gate lengths for minimized leakage devices is the primary challenge at the gate level for SADP levels. Extra gate lengths in SADP patterning often need the use of an additional mask for each additional gate length required. Additional masks are used at the endpoints of the patterned levels in both SADP and SAQP procedures to chop the end spacers. When it comes to area scaling, this is an extra concern. This issue is complicated at the MOL and BEOL wiring levels, where the wire must connect the dense transistors beneath and leave enough space between wiring lines. For the contact and lower wiring levels, this causes the MOL levels to drive to three and four levels of optical patterning.

Additional wire levels have been added as a result of the requirement to maintain diverse wiring lines and the constraint of unidirectional wiring.




Self-Aligned Quadruple Patterning (SAQP) for the FIN level. The steps: a) photoresist patterning b) after 1st spacer and etch c) resist removal d) after 2nd spacer and etch and finally e) 1st spacer removal

For similar transistor density in the design library, this has resulted in a considerable increase in MOL and BEOL wiring levels. In other words, rather than the transistor density below, the library density is restricted by the wiring available in the MOL and BEOL. Design Technology Co- Optimization, or the optimization of design interaction and technology definition, has become an important area of development attention (DTCO). As a result, it's clear to see how device variability and area scaling pressure have enhanced the requirement for lower wavelength imaging.

**C. Transistor formation**

FinFET will most likely be advanced to 7nm by chipmakers. The current control in finFETs is performed by putting a gate on each of the three sides of the fin. However, don't expect any significant changes in material sets at 7nm. Scaling standard silicon-based finFETs to 7nm will be difficult enough for chipmakers. Consider the contacted poly pitch (CPP) in a device. A 14nm finFET typically has a 72nm CPP. Chipmakers want to scale the CPP to 36nm at 7nm. "Material sets will evolve," GlobalFoundries predicts. "The basic difficulty that the sector faces is that the technologies are diminishing." The distance between the gates is clearly narrowing. This is what we'd call a CPP. That shrinkage is reducing the amount of area available for a contact between your gates." There are other issues to consider. "The key challenges for greater performance will be contact resistance reduction and channel mobility improvement,”. "Innovations to minimize parasitic capacitance are also required."

Chipmakers will most likely re-engineer the fin to lengthen the finFET's life. Making the fins taller is one option. Taller fins give greater drive current, allowing for faster chips while using less power, but

they also increase device capacitance. The most likely path is to lower the capacitance by scaling the fin. Both the fin pitch and height might be 30nm in one instance at 7nm. Intel's 14nm finFET, on the other hand, has a fin pitch and height of 42nm. Meanwhile, the industry has been presenting new channel materials to improve device mobility for some time. The options for next-generation channel materials are III-V, germanium (Ge), and silicon germanium, as previously (SiGe). "There's still a long way to go before silicon dies, and for properly scaled Ge or III-V devices to be competitive with silicon," says. "At 7nm, don't anticipate exotic channel materials." SiGe is a channel material that has the potential to be a dark horse contender. It's not brand new, and it's already been employed in planar devices. It provides significant benefits to the PFET. NFET, on the other hand, is the device that requires the most attention."

**D. BEOL (back end of line)**

The BEOL is where a device's interconnects are created. At each node, interconnects—the microscopic wire systems in devices—are becoming more compact, resulting in an undesirable resistance-capacitance (RC) delay in chips. According to a study from the Georgia Institute of Technology, the average delay due to copper resistivity increased by 7.6% from 45nm to 22nm. According to Georgia Tech, the delay is predicted to increase by 21.8 percent from 22nm to 11nm and by 48 percent from 11nm to 7nm. However, there is no straightforward answer to the situation. "As we go away from the 20nm, 10nm, and 7nm nodes, the interconnect is at an inflection point, and the shape it takes will be determined by pitch scaling." "Because everyone scales differently, solutions to well-known high- value interconnect challenges like metal fill, via and line R, capacitance scaling, and reliability management are bucketed by pitch rather than node." Pitch, not node, is now the reference point."

In any event, chipmakers in the BEOL will continue to face a lot of problems. This involves the copper dual damascene technique, which is a standard metallization strategy. Tantalum nitride (TaN) materials are employed for the barrier in a copper dual damascene structure. Cobalt (Co) replaced tantalum (Ta) as the liner starting at 20nm. TaN and Co should be able to scale to 10nm and 7nm, respectively. For good reason, the industry is looking at new materials for the BEOL. "At 7nm and below, the barrier/liner thickness does not scale well, resulting in smaller volume for copper fill and greater resistance," explains. "In addition, due to surface scattering and/or grain boundary scattering, metal resistivity tends to rise at decreasing dimensions." While we anticipate copper will be extended to 7nm and beyond, the road for 5nm and beyond is less clear, therefore we're exploring for ways to extend copper as well as new materials." Low-k dielectrics are another concern. The k- effective number has been locked at 2.4 for years. Scaling low-k films is difficult, in part because of the materials' weak mechanical characteristics. "Low-k scaling is focused on creating films with lower process induced damage to effectively produce lower integrated capacitance for similar bulk film k," stated Applied's Naik. "New materials with enhanced etch stop qualities continue to drive effective k scaling by allowing thinning of the dielectric etch- stop/barrier stack and lowering the fringe capacitance to decrease effective k."

**E. MEOL (Middle-End-Of-Line)**

Tighter CGP has resulted in a more sophisticated and expensive MEOL for Metal-1 to touch the underlying high density of transistors starting at 20 nm [21]. The MEOL, which was previously a single-mask module in 28 nm, now requires well over a dozen masks even at 10 nm. SACs and gate contacts made independently of the finFETs are used to contact them. To allow dense local routing, further levels of local vias (Via-0, gate via, and source/drain via) and metal (Metal-0) are necessary. Each MEOL level requires a high pitch, such as 40 nm for 7-nm Metal-0 [5], necessitating multiple patterning; four masks per 7-nm MEOL level is fairly unusual. MEOL specification is based on a thorough DTCO analysis and

has been fine-tuned to strike a balance between process complexity (yield risk) and logic/SRAM space reduction. Special process structures such as diffusion-to-diffusion jumpers, cross-coupling connections, and single-diffusion breaks, for example, can minimize standard cell space (SDBs).

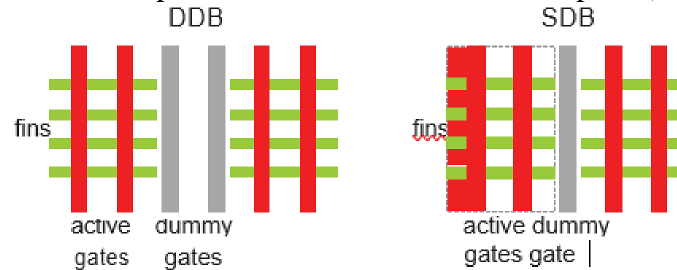



**Fig. 3. Layout view of single vs. double diffusion break By removing dummy gate waste, SDBs can potentially**

save 10% logic area. For improved control of source/drain fin epitaxy in fin-FET fabrication, the end of an active area must terminate at a dummy gate spacer. A double diffusion break (DDB) is required if a narrow shallow trench isolation (STI) cannot be inserted under a single dummy gate and abutted devices cannot terminate on a shared dummy gate. SDB was available as early as the 14-nm node, due to developments in aggressive STI oxide fill.

**F. Technology Parasitics elements**

At 7nm groundrules, the Replacement Metal Gate FINFET device contains substantial parasitic components. It is essential to hyper-regulate various elements in order to control these parasitics and their variability (eg. FIN height, gate height over the FINFET, thermal budgets, contact etches and critical dimensions). Figure 4 below illustrates the situation. The summation of the device channel resistance, the resistance under the spacer (Rsp), and the spreading resistance in the doped Epi region is the intrinsic resistance of the FINFET device (Repi). The resistance beneath the spacer faces several significant obstacles. The height of the FIN will affect any extension implant that supplies dopant from the top surface (for self-alignment under the spacer). This depth dependence is unique to this device structure, and it completely undermines the device's electrostatics. As a result, Rsp and device electrostatics have an inherent tradeoff. Similarly, Repi reduction is accomplished by extensively dosing the Epi. If the dopant travels inside the channel due to further heat processing, this has a negative effect on the device's electrostatics. As a result, multiple layers of Epi with different amounts of dopant are grown to control the Repi. The contact's resistance is determined by the silicide's resistance (which is determined by reducing Rho c) as well as the contact's (CA) and Via's resistance (V0).

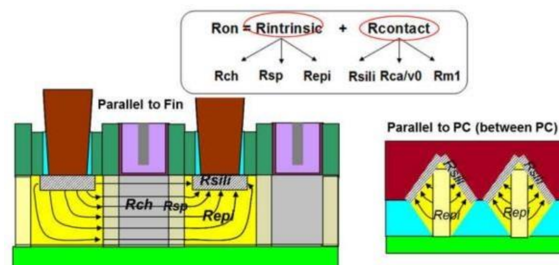



**Figure 4. Resistance components of the FINFET; Left – Parallel to and along the FIN; Right – orthogonal to the FIN.**

sFigure 5 shows the optimization of the various MOL layers. The figure depicts the numerous connections in a plan perspective parallel to the gate (PC). The contacts (CA) must contact and connect the Epi growth from all FINs that make up the device's source/drain. The contact to the Epi and the

contact to the gate (CB) must also be separated.

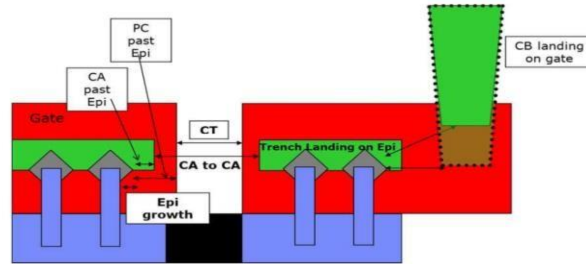



**Figure 5. Factors in the patterning of the MOL wiring levels;**

CT (gate cut), CA is contact; Gate (PC) is shown in red. Gatecontact (CB) is shown to the right. Because of the problematic arrangement of the numerous contacts, multi-level patterning in the MOL has become more complex, and the razor-thin process margin has resulted in high variability. The parasitic components that result are shown in Figure 6. The contacts themselves, as well as the Rho c-driven silicide resistance, are the key detractors. Figure 8 shows how an EUV exposure at the same level improves the distribution of resistance for a via chain when an optical multi-patterned optical exposure level is replaced. EUV clearly aids in the reduction of parasitics in the MOL, and this will be the key rationale for its deployment as soon as it is ready for production. Scaling problems can be found all the way down to the BEOL wire layers.

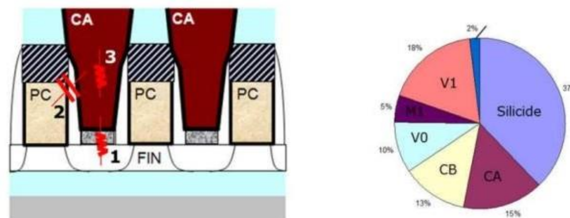



Figure 6. MOL wiring parasitics. On the left 1) contact to Si 2) capacitance to gate and 3) contact resistance; the pie chart on the right shows the contacts and the silicide account for >60% of the resistance components.

**Conclusion**

As we know that today with the improvement in technology the size of semiconductor is getting smaller and smaller. There are lots of benefits and challenges of this new technology. In case of benefits, we can say that by reducing size the power consumption is reduced, switching performance is improved and density is also increase. In terms of fabrication and design there are serval challenges that we have to face like mask making, patterning, transistor forming, BEOL, MEOL, parasitic elements etc. With each successive node, parasitics and layout-dependent impacts will become more prominent. Even though these challenges, the PPA (power, performance, and area) has pushed major semiconductor companies, particularly those involved in the supply chains of mobile, portable, and server processors, to go to 7nm. So here we found that there are serval challenges we have to face while making 7nm Technology. But may be in future people find out it solutions.

**ACKNOWLEDGMENT**

The topic what I discuss here is given by my professor Hongbin Yu (Arizona State University) so I am thankful because after working on this project I learn many thing. Apart from this I am also grateful for

the reference paper thatI used in this project.

**REFERENCES**

1. Alvin L. S. Loke, Da Yang, Tin Tin Wee, Jonathan L. Holland, Patrick Isakanian, Kern Rim, Sam Yang, Jacob S. Schneider, Giri Nallapati, Sreeker Dundigal, Hasnain Lakdawala, Behnam Amelifard, Chulkyu Lee, Betty McGovern, Paul S. Holdaway, Xiaohua Kong, and Burton M. Leary, "Analog/Mixed-Signal Design Challenges in 7- nm CMOS and Beyond". 2018 IEEE Custom Integrated Circuits Conference (CICC).
2. R. Divakaruni and V. Narayanan, "Challenges of 10 nm and 7 nm CMOS for Server and Mobile Applications". IBM Semiconductor Technology Research,257 Fuller Road, Albany, NY 12203, 1101 Kitchawan Road, Yorktown Heights, NY 10598
3. Chang, J.; Chen, Y.; Chan, W.; Singh, S. P.; Cheng, H.; Fujiwara, H.; Lin, J.; Lin, K.; Hung, J.; Lee, R.; Liao, H. (February 2017). "12.1 A 7nm 256Mb SRAM in high-k metal-gate FinFET technology with write-assist circuitry for low-VMIN applications". 2017 IEEE International Solid-State Circuits Conference (ISSCC):
4. Ajey P. Jacob, Ruilong Xie, Min Gyu Sung, Lars Liebmann, Rinus T.
5. P. Lee and Bill Taylor, "Scaling Challenges for Advanced CMOS Devices". International Journal of High Speed Electronics and Systems. Vol. 26, No. 01n02, 1740001 (2017)
6. Rama Divakaruni1 and Vijay Narayanan2, "(Keynote) Challenges of 10 nm and 7 nm CMOS for Server and Mobile Applications". © 2016 ECS - The Electrochemical Society ECS Transactions, Volume 72, Number 4
7. Andrzej J. Strojwas*, Kelvin Doong and Dennis Ciplickas, "Yield and Reliability Challenges at 7nm and Below". 2019 Electron Devices Technology and Manufacturing Conference (EDTM)
8. T. Vasudeva Reddy, K. Madhava Rao, P. Kavitha Reddy, "Design of FinFET based 128 bit SRAM in 7nm & Various Effects near Threshold Operation for Ultra Low Power Application". International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277- 3878, Volume-8 Issue-5, January 2020
9. MARK LAPEDUS, "7nm Fab Challenges". Semiconductor Engineering. APRIL 21ST, 2016
10. Mohit Bansal, "The benefits and Challenges for 7nm node tecchnology". Blog from wipro. February 2020.