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Optimizing Energy-Efficient in VLSI Architecture for FIR Filter in Seismic Signal Processing

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Abstract
This project aims to developing an optimized and energy-efficient VLSI design for FIR filters specifically designed for seismic signal processing. The process begins by converting seismic signal dataset values into binary format, and then, simulating them in MATLAB, and generating a coefficient file. This coefficient file is then analyzed using Verilog HDL code and simulated in the Xilinx Vivado 2022.2 tool to assess key parameters such as area, delay, and power. The suggested architecture lessens the complexity of computing, hardware efficiency compared to traditional FIR filters that utilize the CSE technique. This design employs a critical method known as the CSD-based Matrix-Grouped Common Subexpression Elimination (MCSE) algorithm, which significantly reduces the quantity of logic operators (LOs) and logic depths (LDs). Additionally, the design incorporates a Half-Unit Biased (HUB) rounding technique to minimize the truncation errors and cut-set retiming method to reduce the critical-path delay (CPD). This hardware-efficient FIR filter constructs integrates the CSD-based MCSE algorithm, HUB rounding, and cut-set retiming techniques to offer a reconfigurable FIR filter configuration optimized for hardware efficiency, thereby enhancing the real-time alert seismic signal processing. The implementation of an Artix-7 FPGA board including clock gating techniques to further reduces the power consumption.

Index Terms: Finite Impulse Response (FIR), Half-Unit Biased (HUB), Canonical signed digit (CSD) based matrix groped Common Sub-Expression Elimination (MCSE), Seismic Signal, Clock Gating.

I. INTRODUCTION

In digital FIR filters to removing noise from seismic signals is a pivotal challenge in seismic signal processing, especially for seismic alert systems (SAS). Digital finite impulse responses filters are commonly utilized in these applications due to their linear phase features and reliable performance. Nevertheless, the large amount of multiplying and addition operations needed for standard FIR filter designs sometimes causes problems with extended calculation times, excessive size and power consumption, and other additional matters. In particular, they are essential for real-time applications of programs. Consequently, there has been an increased focus on refining FIR filters design using techniques like Common Sub-expression elimination (CSE) to lower area utilization, power consumption, and latency. In order to create effective multiplier-less FIR filters and reconfigurable architectures, recent advancements have proposed hybrid CSE approaches. These techniques use an MCSE algorithm based on Canonical Signed Digit (CSD) to significantly reduces the hardware costs. In real-time, sensor-based

systems, SAS must provide a rapid speed, little energy low-pass FIR filter architecture to enable quicker processing and early alerts while preserving power. The goal of this project is to create a FIR filter structure that is optimized in terms of size, latency, and power efficiency so that seismic signals may be precisely and instantly pre-processed.

The goal of this research is to create an area, delay, and power efficient FIR filters architecture designed for pre-processing seismic signals in real-time alert. The fundamental concepts are of:

1. Novel MCSE Algorithm: Presenting a new matrix-grouped Common Subexpression Eliminations (MCSE) algorithm designed to reduce computational load and achieve greater optimization in reducing (LO) and (LD) compared to traditional CSE methods.
2. High-Speed, Low-Power FIR Filter: Developing a high-speed, low-power systems response filters for finite impulses sfor seismic signals pre-processing, utilizing CSD-coded filter coefficients in combination with the MCSE technique and a Half-Unit Biased rounding method to minimized the truncation errors, cut-set retiming technique to decreases the CPD and fixed-point rounding format to enhances the power efficiency, while adder tree retiming boosts processing speed, leading to an architecture that outperforms current solutions in seismic applications.
3. Reconfigurable Filter Architecture: Designed to addresses the basic real-time applications entail that require dynamic adjustment of filters coefficients, the proposed architecture, MCSE algorithm help in phone line server to provides flexible adaptation to varying signal conditions. It outperforms current state-of-the-art solutions by lowering hardware complexity and Critical Path Delay.
4. MCSE Algorithm for Noise Filtering: During the filtering phase with each other, the algorithm efficiently lowers the processing burden. making it especially advantageous for applications like speech enhancement. By grouping similar operations and reusing intermediate results, it minimizes interference signals and enhances voice quality, leading to faster processing and decreased resource consumption.

Additionally, the effectiveness of the MCSE algorithms is validated through comparative testing against benchmarks, showing significant improvements in measures for excellence such as Word Recognition Rate (WRR) across various noise environments. For example, the MCSE algorithm achieves higher WRR percentages than baseline models in stationary noise conditions, demonstrating its superior efficiency in noise reduction tasks. Overall, the MCSE algorithms to reduces computational load by efficiently managing common sub-expressions, resulting in optimized performance in noise filtering applications.

1. Basic structure of Finite impulse response Filter

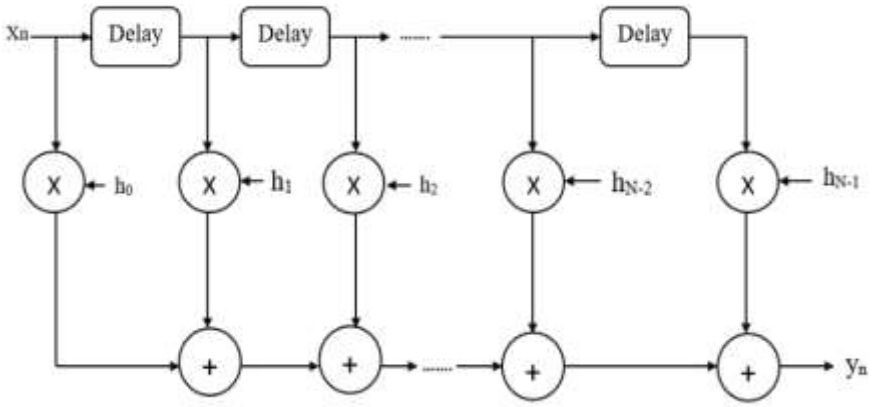

Fig 1: The Logical structure of an FIR filter

The Basic structure of (FIR) filter consists of:

1. Input Signal (x[n]): The input signal to the FIR filters is represented as x_n.
2. Delays**:** The blocks labeled "Delay" represent unit delays. Each delay block stores the current input sample and passes it to the next stage at the next clock cycle. This creates a series of delayed input samples.
3. Multipliers (×)**:** The circles with "×" are multipliers. Each delayed input sample is multiplied by a corresponding filter coefficient h_k. These coefficients represent the FIR filter's characteristics, which determine the filter's frequency response.
4. Adders (+)**:** The circles with "+" are adders. The valuess of the multipliers (delayed input samples multiplied by filter coefficients) are summed together. This sum is the output of the FIR filters at the current time step.
5. Output Signal (y[n]): The final sum of the products is the output signal y_n

The fig 1 illustrates the working of an FIR filter, which processes an input signal x[n], by passing it through a series of stages involving delays, multipliers, and adders. Each stage introduces a delay, effectively creating a series of past input samples. These delayed samples are then multiplied by fixed filter coefficients h_k. The products of these multiplications are summed to produce the filter's output y[n].

1. Mathematical Function of FIR filter:

The output of an Finite Impulse Responses filter expressions are possible by the convolution sum:

$$y[n] = \sum_{k=0}^{N-1} h[k] \cdot x[n-k]$$

Where:

- y[n] is the output signal at time n.
- x[n] is the input signal at time n.
- h[k] are the filter coefficients (impulse response of the filter).
- N is the quantity of filter coefficients.

2. Basic shift and adder-based method

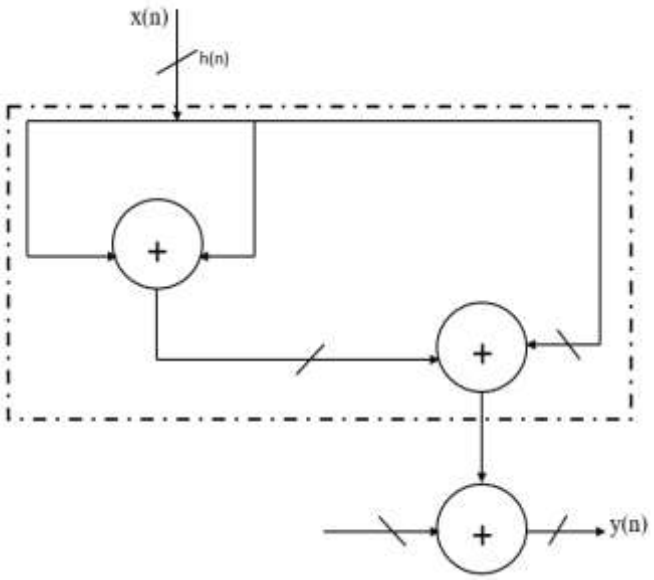

Fig 2: Shift and adder-based Method

The shift and adder structure involves the input signal x[n] being processed through a series of multiplications with filter coefficients h[n]. The intermediate products are then summed by the adders to produce the desired result signal y[n].

3. CSD based Matrix grouped CSE method

This method aimed at optimizing FIR filter architecture designed by minimizing the amount of adders and multipliers. In Below detailed explanation of its working:

a. Canonical Signed Digit (CSD) Representation:

It is a method used to reduces the numbers of non-zero digits (1s) in binary numbers, which in turn shrinks the quantity of addition and subtraction required in digital computations. In the context of FIR filter, this contributes in optimizing the hardware implementation by lowering the complexity.

b. Operation of Matrix Grouped Common Subexpression Elimination (MCSE):

Common Subexpressions Elimination (CSE) is a technique used to identify and eliminate redundant calculations in digital signal processing. The matrix-grouped CSE approach improves upon this method by arranging filter coefficients into matrices and applying CSE to detect common subexpressions both vertically and horizontally.

c. Working of the CSD-Based Matrix Grouped CSE Method:

1. Binary and CSD Conversion: The filter coefficient are first starts by converting into binary form. In the case of significantly greater coefficients negative, two's complement Representing has been used.
2. Vertical CSE (VCSE): In the initial stage, with Vertical CSE is applied to the binary coefficient. This involves examining the coefficients column by column to identify and eliminate common sub-expressions. For instance, if multiple coefficients share same bit patterns at identical bit locations, those patterns are noted and reused to minimize redundant calculations.
3. Horizontal CSE (HCSE): After the VCSE is applied, This involves looking across the coefficient row by row to find common sub-expression. The process begins with smaller groups of bits (e.g., 3 bits) and then moves on to larger groups (e.g., 6 bits). By eliminating common subexpressions horizontally, further redundancy is minimized.
4. Grouping and Optimization: The coefficients in grouped into sets, and within each set, CSE is utilized to maximize the reuse of common sub-expression, This step is crucial in decreasing the amount of adders required.
5. Reduction in Adders and Multipliers: By employing both vertical and horizontal CSE methods along with CSD depiction, an enormous reduce in the quantity of adders and multipliers required is achieved, which results in a more hardware-efficient design for FIR filters, further reduced power applied for clock gating technique.

The structure of this document is as follows:

Section II : Brief about Literature Survey.
Section III : Proposed Methodology.
Section IV : Present the simulation and synthesis results.
Section V : Conclusion
Section VI : References

II. LITERATURE REVIEW

Sudipta Bose Arijit De and Indrajit Chakrabarti, [1] This study looks at to improve FIR filter construction

for real-time seismic alert systems, A (HUB) rounding procedure and a novel matrix grouped CSE (MCSE) method have been offered, and approach to cut-set retiming method. This methods reduces hardware complexity, critical-path delay (CPD), and truncation errors. Two hardware-efficient architectures, implemented on FPGA and ASIC platforms, demonstrate significant reductions in logic operators, CPD, area-delay-product (ADP), and power-delay-product (PDP) compared to existing CSE-based architectures, making them well-suited for applications that requires real-time processing.

A.Chandra and S.Roy, [2] This short presents a novel triangular (CSE) algorithm that eliminates repetitive bit patterns, hence reducing the total amount of logic operators (LOs) in filtering with FIR. This strategy minimizes logic depths and logic operators far superior to current CSE techniques. Implementing the concept on a Cyclone IV FPGA chip validates its effectiveness, and results from simulation demonstrate a substantial decrease in LOs.

I. Sharma, A.P Kumar, L. Balyan, and G. K. Singh, [3] In order to achieve finite impulse response, or FIR, the present research aims to minimize the entire amount of adders in digital filter designs. This work adds to earlier efforts by suggesting a way to lower the amount of processing needed in filters that employ FIR for various purposes. The proposed method combines vertical and horizontal common subexpression eliminating (CSE) strategies to produce filters that maintain significant characteristics while significantly reducing the necessary number of adders.

I. Hatai, I. Chakrabarti, and S. Banerjees, [4] The Vertical-Horizontal The binary Common Subexpression Eliminations (VHBCSE) approach is employed in this paper's fixed multiplier design to create reconfigurable (FIR) filters with variable coefficients. The 2-bit binary common subexpressions are eliminated vertically across neighboring coefficients by the VHBCSE method, while the variable-bit subexpressions are eliminated horizontally inside individual coefficients. Compared to other techniques, this one dramatically lowers flipping activity and energy usage in the factors(multiplier) block adders. The area-power product (APP) and power-delay product (PDP) exhibit improvements in the ASIC implementation accomplishments, demonstrating the algorithm's efficacy in synthesizing fixed-point reconfigurable FIR filters.

R. Mahesh and A.P Vinod, [5] This study provides a new CSE approach to enhance the design of linear-phase finite impulses response filters by using binary coefficients. By utilizing fewer adders in the multipliers effects, this approach optimizes effectiveness over conventional CSE methods that employ canonical signed digits (CSD), particularly in higher-order FIR filters. Using binary coefficients, the algorithm reduces the amount of unpaired bits without increasing the logic depth or significant route length, resulting in an average adder decrease in 18% as opposed to existing methods.

S.-F. Hsiao, J.-H. Z. Jian, and M.-C. Chen, [6], This work discusses filter with finite impulse responses (FIR) designs that are both economical and efficient by using reduced multipliers that are authentically rounded. Bit width and hardware resources are optimized while maintaining output signal accuracy and response frequency accuracy. By using nonuniform coefficient quantization and carefully choosing the filtering sequence, the overall area cost is decreased. The direct FIR structure incorporates an improved version of truncated multipliers for many times at constant multiplication and accumulation. Compared to previous FIR design techniques, the offered alternatives have improved area efficiency and reduced energy consumption.

S. J. Lee, J. W. Choi, S. W. Kim, and J.I Park [7], This work presents a low-power reconfigurable FIR filter designed that optimizes efficiency for fixed filter orders. To become involved in negotiations energy and efficiency savings, the design continuously adjusts the filters positions according to coefficients and

the frequency range of the input data. Comparing to conventional methods, mathematical analysis and practical findings indicate that an area surplus of less than 5.3% with power reductions up to 41.9% may be obtained with no compromise in performance.

IV. PROPOSED METHODOLOGY

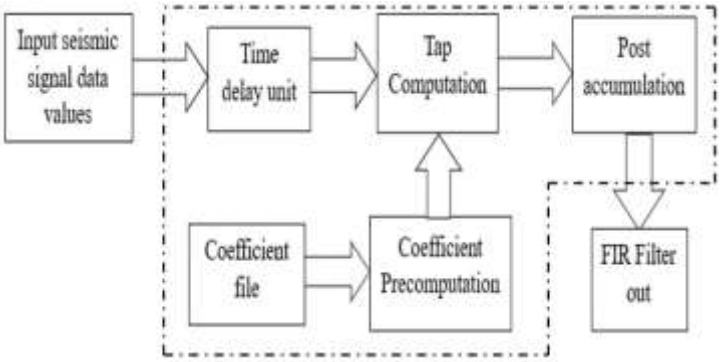

Fig 3: Flow diagram of Proposed Method

Proposed Flow diagram explanation given below

- **Input seismic signal data values:** Represents the raw seismic signal data values that will be processed by the matlab. The data is converted into binary format during preprocessing and serves as the starting point for the filtering process.
- **Time delay unit:** An introduces necessary delays to the signal received samples, enabling the filter to access previous signal samples. This unit is crucial for the convolution operation performed by the FIR filter, as it aligns the input samples with the corresponding filter coefficients.
- **Coefficient file:** This file generated in matlab for precomputed filter coefficients. The coefficients define the filter's frequency response and are used in the tap computation process.
- **Coefficient precomputation:** The optimizes the utilizes the CSD-based Matrix-Grouped Common Sub-Expression Elimination (MCSE) algorithm to precompute partial products and identify common sub-expressions among the coefficients. This optimization minimizes the quantity of logic depths (LDs) and operators (LOs), leading to a more efficient hardware Implementation.
- **Tap computation:** The Tap Computation block performs the actual multiplication of delayed input signal data values samples by the corresponding filter coefficients. Each product represents a "tap" in the filter. This block typically involves a series of multipliers.
- **Post accumulation:** Accumulates the results from the tap computations to form the final filtered output. The use of Half-Unit Biased (HUB) rounding method, helps minimize the truncation errors and cut-set retiming technique for reduce critical path delay, ensuring accurate and precise output.
- **FIR filter out:** The final output of the filter, which is a processed version of the seismic signal input. This output is used for further analysis or applications in seismic signal processing.

To further optimize the filter for reduced hardware complexity and efficiency, the clock gating method is applied.

Clock gating technique

In VLSI circuit design, minimizing power dissipation becomes increasingly important as technology

scales down, which often results in higher power leakage. Traditionally, optimization efforts have focused on factors such as area, delay, and testability. However, to effectively reduce power dissipation, approaches such as clock gating
employed. By interrupting the clock signal to inactive circuit components, clock gating lowers dynamic power usage. By limiting signal activity, our suggested design focuses on lowering dynamic power dissipation and saving energy by gating the clock when it's not needed.

Latch based clock gating method

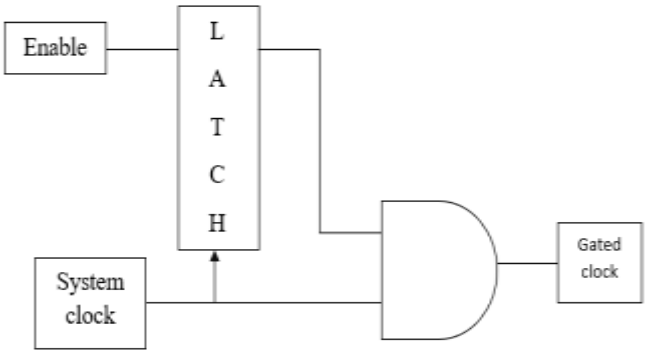

Fig 4: Latch based clock gating diagram

The latch-based clock gating approach is a power-saving method used in digital circuits, particularly in VLSI design. It reduces power consumption by selectively enabling or disabling the clock signal to various parts of a circuit according to the system's requirements. The primary components involved in this method.

1. Enable Signal: This control signal controls whether or not the clock signal is sent to the gated clock output. It serves as a prerequisite for turning on or off the clock.
2. Latch: The latch captures the state of the enable signal at a specific time, ensuring that the enable condition is stable and reliable before it affects the clock gating. This helps in avoiding glitches that could occur if the enable signal changes rapidly.
3. System Clock: This is the primary clock signal used in the system. The system clock is the reference clock signal that drives the timing of the entire circuit.
4. AND Gate: The AND gate combines the system clock and the output of the latch to generate the gated clock. If both the system clock and the enable condition are active, the gated clock is generated.
5. Gated Clock: This is the output clock signal that is either enabled or disabled in accordance with the system clock and the enable signal. The specific circuit components that require activation or deactivation are driven by the gated clock.

Latch-based clock gating is a power-saving technique that controls when a clock signal reaches a circuit block. It uses a latch to store the enable signal, ensuring it's stable during the clock's active edge. This prevents glitches and maintains proper clock pulse width. An AND gate combines the latch output with the system clock, creating a gated clock that only passes when both signals are high. This way, the clock is only active when the circuit block needs to operate, reducing power consumption.

Application

1. **Seismic monitoring and early warning systems:** The architecture can be applied to build sophisticated early warning and seismic monitoring networks. These are necessary instruments for

detecting earthquakes and tsunamis so that vulnerable people may be properly evacuated.

2. **Oil and gas exploration:** In Advanced seismic monitoring networks and early warning systems may be created using this architecture. These advances in technology are essential for detecting earthquakes and tsunamis. so that communities at danger can be promptly alerted.

V. SIMULATION AND SYNTHESIS RESULTS

The developed the Verilog HDL code for CSE design consists of LO and LD minimization method design entry, simulation and synthesis. The Proposed Architecture CSD based matrix grouped CSE(MCSE) algorithm has been coded in Verilog Language and verified their functionality using XILINX VIVADO 2022.2 simulator. Once the functional verification is done, The RTL model is taken to the synthesis process, where the optimized netlist is viewed and Area, power and delay etc is obtained. These parameter area, power and delay etc are compared with my base implementation.

Consequently, the processed output in power will be reduced and my Proposed method but delay will be same in both the method. The simulated and synthesized results as follows..

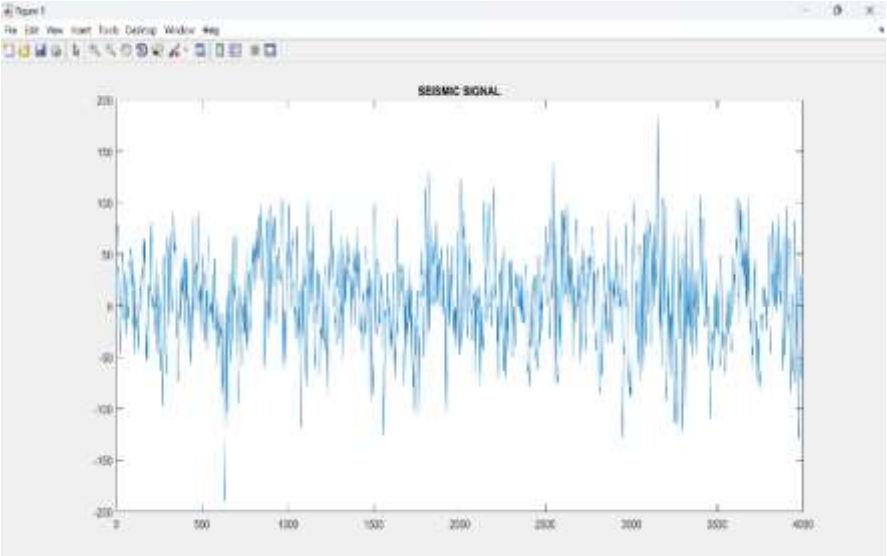

Fig 5: Seismic signal result in matlab

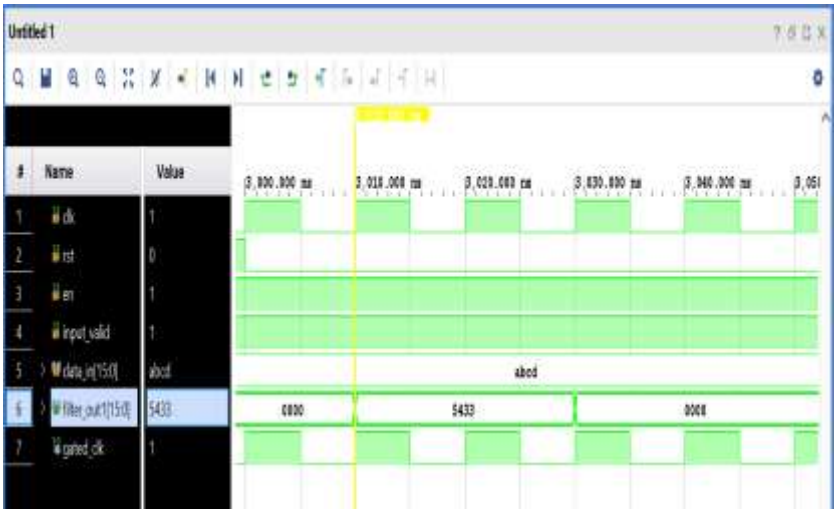

Figure 6: Simulated waveform for FIR filter

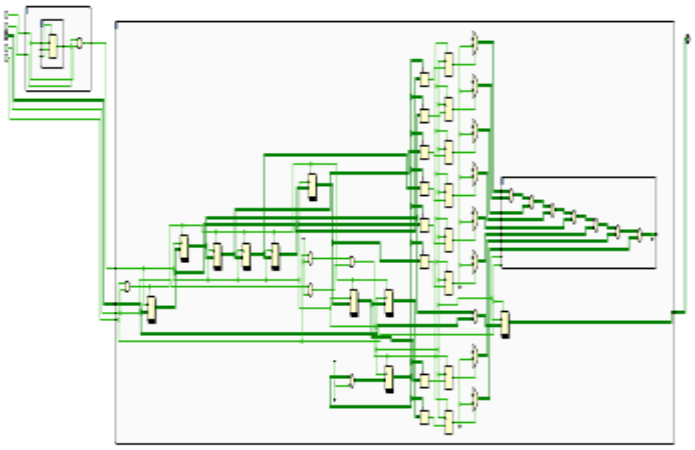

Figure 7: RTL elaborated design for FIR filter

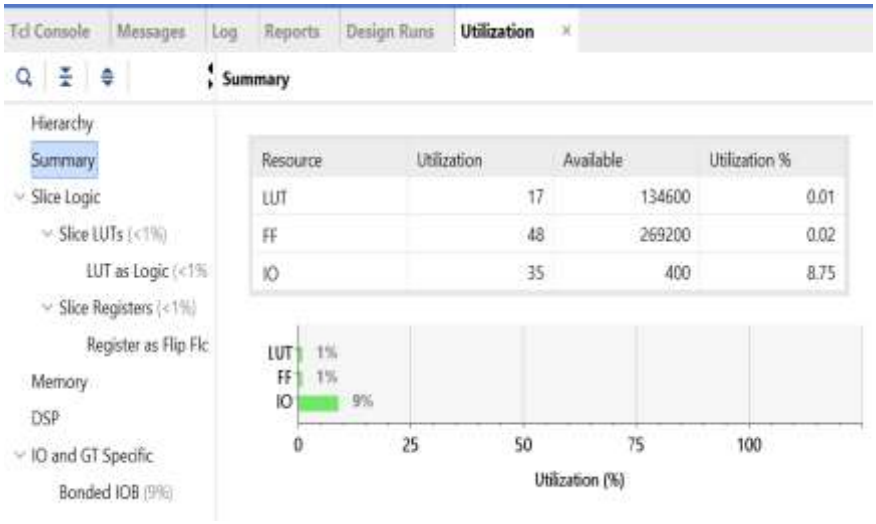

Fig 10: Area report for base method

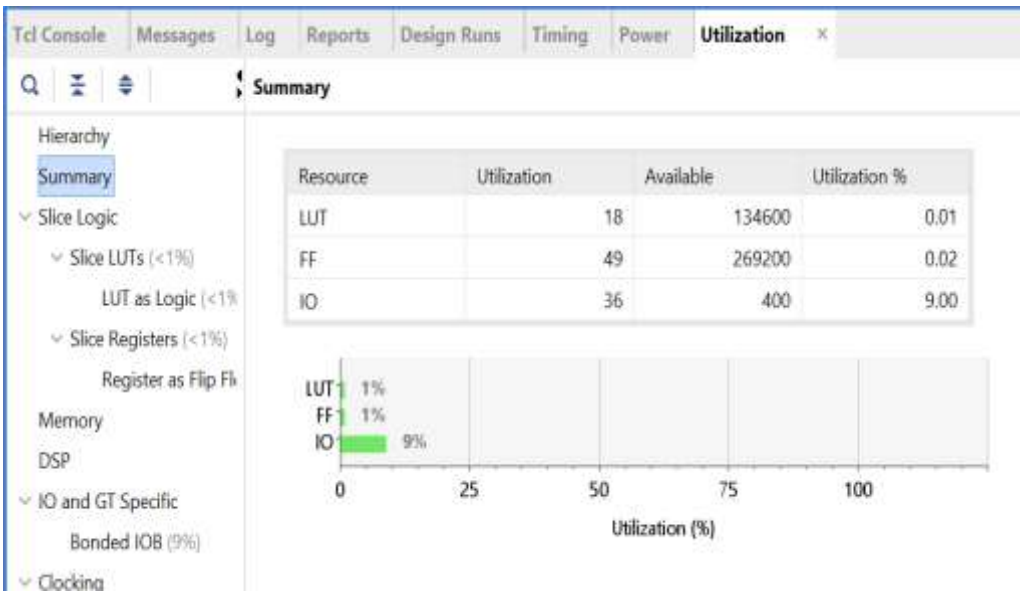

Fig 9: Area report for proposed method

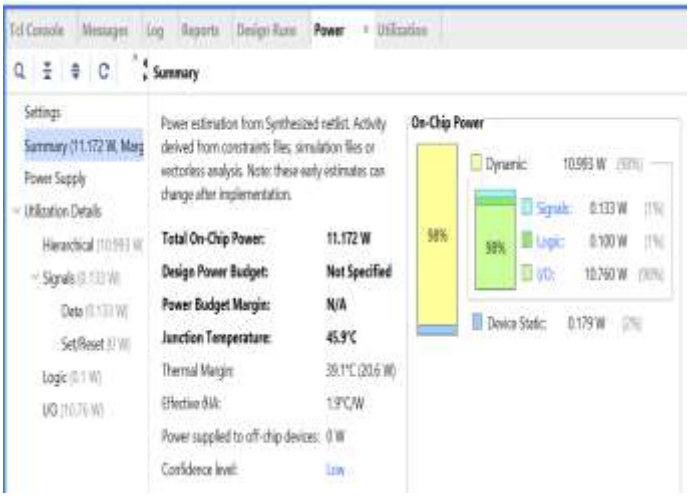

Figure 12: Power report for base method

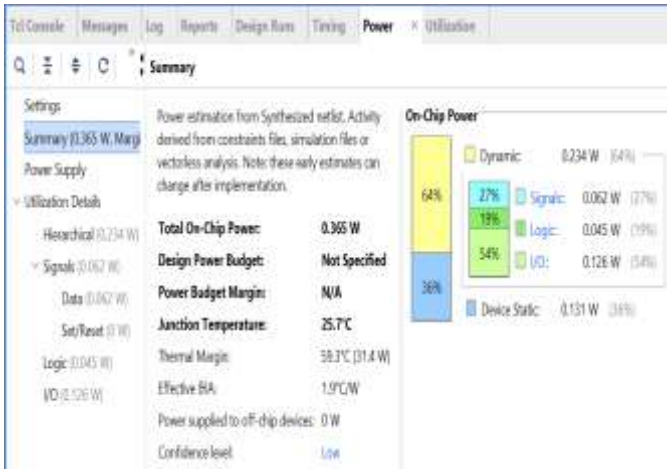

Figure 12: Power report for proposed method

Criteria	Base method	Proposed method
Power(w)	11.172	0.365
Delay(s)	3.521	3.521

Table 1.1: Comparison table between (Base method and Proposed method)

V. CONCLUSION

This project successfully developed and optimized an energy-efficient VLSI architecture for FIR filters specifically designed for seismic signal processing. By employing the CSD-based Matrix-Grouped Common Subexpression Elimination (MCSE) algorithm, the design achieved significant reductions in computational complexity, the number of logic operators, and logic depth compared to traditional FIR

filters. The integration of the Half-Unit Biased (HUB) rounding technique minimized truncation errors, while the cut-set retiming method effectively reduced critical-path delay, ensuring enhanced hardware efficiency and real-time processing capabilities. The architecture's reconfigurability, combined with its implementation on an Artix-7 FPGA board, to demonstrated substantial improvements in power consumption through the use of clock gating techniques. These advancements confirm the suitability of the suggested architecture for real-time seismics signal processing applications, providing a robust, energy-efficient solution that meets the demands of modern VLSI systems.

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