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Innovative Multi-Bit Test Pattern Generators with Variable LFSR Selection Mechanisms

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Abstract
Test Pattern Generators is an important module for testing Asynchronous circuits that guarantee fault detection. In this paper a multi-bit TPGs with tunable LFSR lengths is presented. Our method enables smooth transitions between various word lengths by dynamically selecting LFSR configurations based on control signals. For 4-bit to 7-bit combinational circuits, we have derived a polynomial-based LFSRs and shown effect of stuck-at-fault detections through extensive testing. It includes a discussion of instructional insights regarding fault coverage and digital circuit design. By bridging fixed and flexible BIST solutions, our adaptive TPG design improves fault detection capabilities.

Keywords: BIST, TPG, LFSR, Multi-Bit

1. Introduction

Built-in self-test (BIST) designs are essential for guaran- teeing the dependability and caliber of integrated circuits in the field of digital circuit testing. Chips can diagnose malfunctions while they are operating thanks to these self- contained test structures, which minimize production costs and the requirement for external test equipment. The Test Pattern Generator (TPG) is a crucial component of BIST systems that plays a vital role in producing test vectors that challenge the circuitry and identify possible flaws. This work explores the construction and analysis of multi-bit TPGs, with an emphasis on how well they adjust to different word lengths. We study TPGs that are based on Linear Feedback Shift Registers (LFSRs), which are the pseudo-random pattern gen- erators underneath. Through the dynamic selection of LFSR configurations in response to control inputs, we are able to adapt to various bit lengths. Our TPG architecture is dynamic in part because of the way multiplexers, comparators, and flip- flops interact with one another. Our research attempts to offer instructional insights into fault detection techniques, digital circuit design, and the trade-offs related to multi-bit TPGs. We thoroughly test our designs with both stuck-at and cut faults, proving the effectiveness of fault covering. We also address constraints and practical issues, opening the door for additional study and optimization. We explore the theoretical underpinnings, design tenets, and experimental outcomes of our multi-bit TPGs in the sections that follow. This voyage will take us through adaptive BIST designs, which combine fault detection, polynomial equations, and XOR gates to improve the dependability of digital systems.

2. RELATED WORK

In order to maximize fault coverage, especially with regard to path delay faults, the fundamental idea is to enhance the clocking mechanism of LFSR seeds. The LFSR seeds are put through more iterations by adding extra clocking cycles, which results in a more thorough examination of possible errors, particularly those connected to route delays inside the circuit. [1] A creative method for creating a low-power test pattern generator meant especially for applications like Built-In Self-Test (BIST). The suggested generator optimizes power usage while preserving efficient test coverage by using a modified clock strategy. The generator is suited for use in areas with limited power because it strikes a compromise be- tween power efficiency and test quality through careful timing mechanism adjustment. The study emphasizes the significance of power-aware design strategies in contemporary BIST im- plementations. [2]. Provide a thorough method for creating a test pattern generator that uses little power for Built-In Self-Test (BIST) applications. The suggested generator seeks to provide effective test pattern creation while minimizing power usage. The generator achieves a considerable decrease in power consumption without sacrificing test coverage or pattern generation speed because to meticulous architecture and circuit-level improvements. Advances the current endeav- ors to provide integrated circuit testing solutions that are energy-efficient. [3]. Examinations on how to calculate the characteristic polynomials of Linear Feedback Shift Registers (LFSRs) for deterministic test pattern creation that is inte- grated into the system are made.Investigation on a range of methods and algorithms for effectively deriving characteristic polynomials, which are essential for producing excellent test patterns. Through enhanced polynomial calculation efficiency, the suggested techniques allow for more efficient use of LFSRs in built-in self-test (BIST) applications. [4]. A similar provides a thorough design and analysis of a D flip-flop-based low- power test pattern generator. They provide a unique design that takes advantage of the built-in properties of D flip-flops to achieve notable power savings without sacrificing effective test pattern creation. The efficiency of the suggested generator in reducing power consumption without compromising test quality is proven by thorough study and simulation. [5]. A low-power test pattern generator that utilizes low-transition Linear Feedback Shift Registers (LFSRs) is revealed in the study that is being presented. The suggested generator aims to lower power consumption by utilizing the intrinsic qualities of LFSRs, which are defined by low transition counts. Significant power consumption reductions are accomplished by means of careful architectural design and optimization techniques, all the while guaranteeing the continuous effectiveness of test pattern creation. [6]. Exploring the theoretical underpinnings of SAT-based test generation techniques. [7] It examines sev- eral methods for fault simulation and test design to efficiently detect and model flaws in combinational logic circuits. [8]. In order to effectively identify and simulate defects in com- binational logic circuits, the study explores several ways for fault simulation and test creation. The authors assess several strategies' efficacy in terms of computing efficiency and fault coverage through theoretical analysis and hands-on testing. The significance of robust testing procedures in guarantee- ing the functionality and dependability of digital systems is highlighted in the paper's discussion of the consequences of fault simulation and test creation for overall design verification and validation processes. [9] In order to minimize test data volume and test application time while preserving good fault coverage, the study looks into methods for compressing and compacting test patterns created for scan designs. The authors aim to reduce the resources needed for testing LSIs, which will lower test costs and increase overall testing efficiency, by optimizing the creation and deployment of test patterns.Test data

volume, test application time, and total test expenses are reduced by using theoretical analysis and experimental testing to assess the efficacy of test compression and compaction procedures. The outcomes illustrate the importance of these approaches in the context of contemporary semiconductor production and show how they may be useful in simplifying the testing procedure for LSIs. [10].

3. Basic architecture of Built-In Self-Test (BIST) and Linear Feedback Shift Registers (LFSRS)

Due to the increasing complexity and integration of semiconductor components, it is critical in modern integrated circuit (IC) design to ensure the durability and operation of complex digital circuits. Traditional testing approaches, which rely on external test equipment and long test procedures,may be unsuitable for large-scale production and deployment scenarios. This limitation has led to the development of alternate methodologies, such as Built-In Self-Test (BIST), to solve the issues of testing integrated circuits. BIST is a technique for integrating testing capabilities directly into the IC, reducing the need for external test equipment. BIST allows for complete testing of the IC's operation by embedding test pattern generators (TPGs), signature analyzers, and other test circuitry inside the chip. This method simplifies testing throughout both the production and operation phases, enabling the discovery of errors and defects in the IC's internal components. The Linear Feedback Shift Register (LFSR) is a critical component in many BIST implementations. An LFSR is a shift register in which the input bit is dictated by a linear function of the preceding state. An LFSR uses a feedback polynomial to generate a pseudo-random sequence of bits. LFSRs are preferred for test pattern creation in BIST due to their simplicity, speed, and predictability. LFSRs provide pseudo-random test patterns that cover the whole input space of the IC, allowing for effective functionality testing and the identification of potential faults or defects. Furthermore, the deterministic nature of LFSRs enables repeatability in test pattern generation, resulting in consistent and trustworthy testing results throughout several test cycles. Overall, integrating BIST methods and LFSRs into IC design is critical for ensuring the reliability and functionality of complicated digital circuits. By allowing complete testing directly within the IC, BIST improves the efficiency and efficacy of the testing process, ultimately adding to the overall quality and dependability of integrated circuits in a variety of applications.

4. Implementation and results

The Test Pattern Generator (TPG) is an essential instrument in the field of integrated circuit (IC) testing. Its principal goal is to generate a broad set of test patterns that are required for carefully testing the IC's circuitry. By doing so, the TPG allows for a thorough evaluation of the IC's operational capa- bilities, which is critical in discovering any faults or defects that may jeopardize the IC's functionality. Linear Feedback Shift Registers (LFSRs),To accomplish this, Linear Feedback Shift Registers (LFSRs) are used as the primary method for test pattern generation. LFSRs are preferred because of their efficiency and effectiveness in creating test patterns. Each LFSR is precisely created using a distinct feedback polynomial that is carefully selected based on the intended bit length. This adjustment guarantees that the test patterns generated meet the specific testing needs. Common feedback polynomials used include $x^4 + x + 1$, $x^5 + x^2 + 1$, $x^6 + x + 1$, and $x^7 + x + 1$, each chosen to optimize fault coverage during testing.

Dynamic LFSR Selection Logic

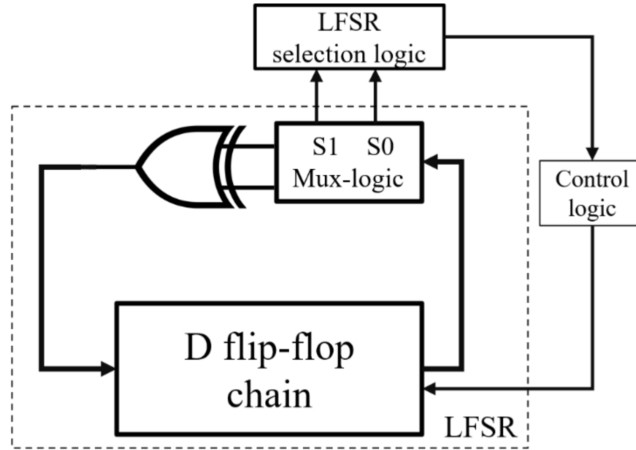

Fig. 1: Multi-bit LFSR

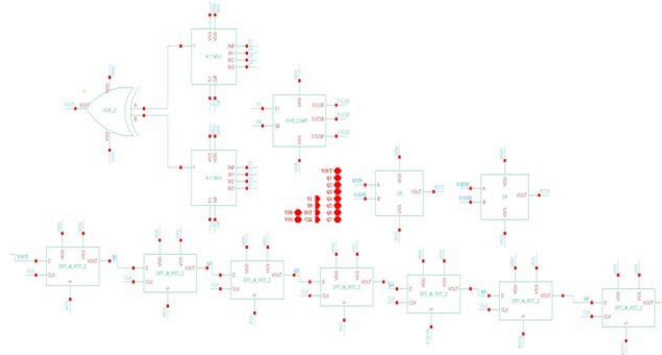

Fig. 2: Schematic of Multi-bit LFSR

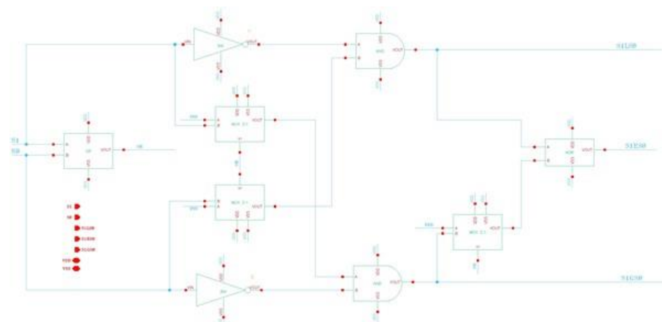

Fig. 3: Control logic

From the above block diagram shown in fig 1, The dynamic nature of LFSR selection is determined by control signals, notably s1 and s0. These signals help determine the length of the LFSR that will be used to generate test patterns. Depending on s1 and s0, the system can choose between 7-bit, 6-bit, 5-bit, or 4-bit LFSRs.The internal operation is shown in the above fig 2 , Adaptive Test Pattern Output via Multiplexers, the Multiplexers play an important part in the dynamic selection process. They are in charge of picking the appropriate output

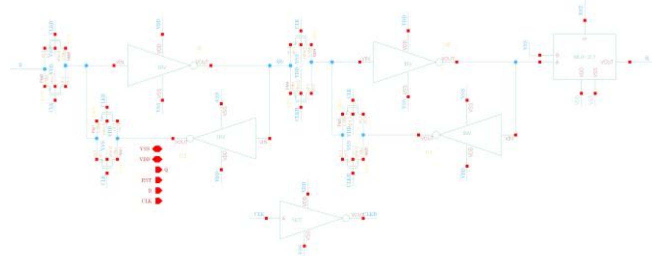

Fig. 4: Synchronous D-Flip flop]

from the LFSR based on the present condition of the control signals (s1 and s0), whose logic is shown in fig.3 The output thus selected is then used as the input test pattern for the next round of testing and the schematic of synchronous D- flioflop is shown in fig 4. Test Phase and Fault Scenarios, During the testing phase, the TPG is rigorously evaluated against various fault scenarios. These include cut faults, which simulate open or shorted connections within the IC, and stuck- at faults, which occur when a signal is incorrectly set at a given logic level (0 or 1). In the absence of any defects, the TPG is supposed to generate pseudorandom patterns that correspond to the predicted outputs for the selected LFSR configuration. Any differences between expected and actual output patterns indicate that the IC may have a defect.

5. Results for Multi-Bit TPGs with Dynamic LFSR Selection

The TPG's efficiency is assessed by its fault coverage, which is determined by intentionally generating issues and then watching the ensuing TPG outputs. Any variations between the predicted and actual patterns are interpreted as indications of potential defects inside the IC. The dynamic LFSR selection process demonstrates the system's versatility, since it can accept different word lengths. This adaptability substantially increases the versatility and flexibility of the Built-In Self- Testing (BIST) architecture. By seamlessly combining fixed and flexible BIST technologies, our technique significantly increases memory system stability. Frome fig 5 to fig 24 shows the results of LFSR with 4,5,6 and 7 input CUT and waveforms and comparison tables of faultfree and faulty CUT.

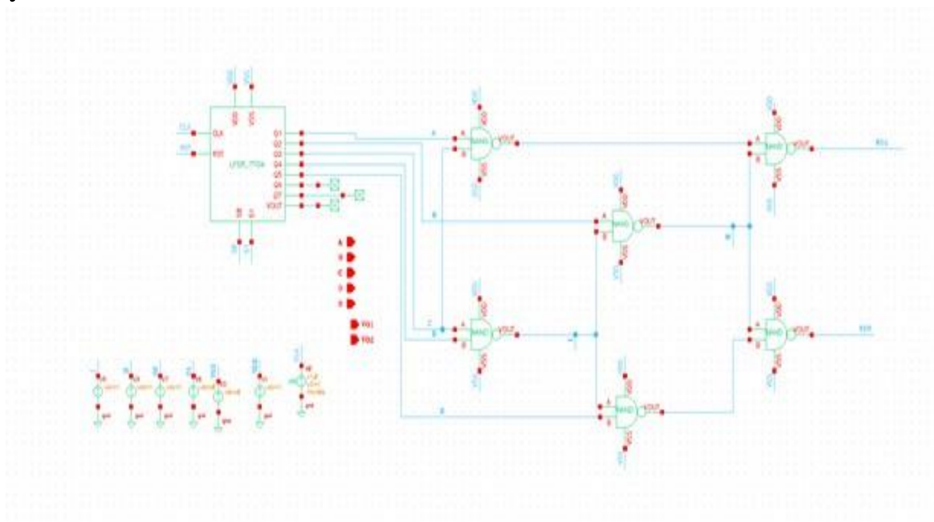

Fig. 5: LFSR with 4 input CUT with labled position 1 and 2

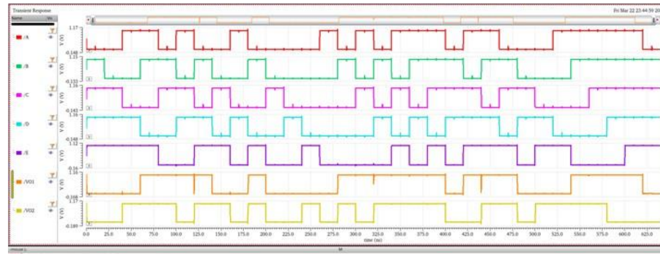

Fig. 6: Waveform for 4 input faultfree CUT

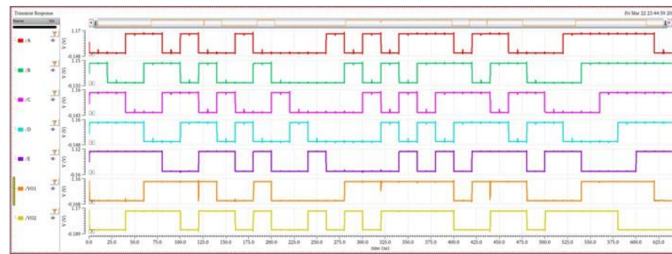

Fig. 7: Comparison table of 4 input faultfree CUT

SI No.	A	B	C	D	VOUT Calculated	VOUT Actual
1	1	1	0	0	0	0
2	1	1	1	0	1	1
3	1	1	1	1	1	1
4	0	1	1	1	0	0
5	1	0	1	1	0	0

Fig. 8: Waveform for 4input Struck at fault 1 at pos1 and 2

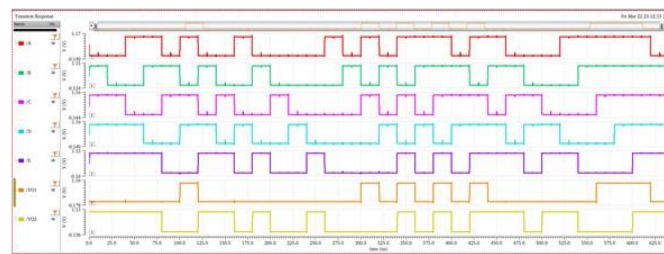

Fig. 9: Comparison table of 4 input faulty CUT i.e.,Struck at fault 1 at pos1 and 2

SI No.	A	B	C	D	VOUT Calculated	VOUT Actual	VOUT Fault free
1	1	1	0	0	1	1	0
2	1	1	1	0	1	1	1
3	1	0	1	0	0	0	0
4	1	1	0	1	1	1	1
5	0	1	1	0	0	0	0

Fig. 10: LFSR with 5 input CUT with labled position 1 and 2

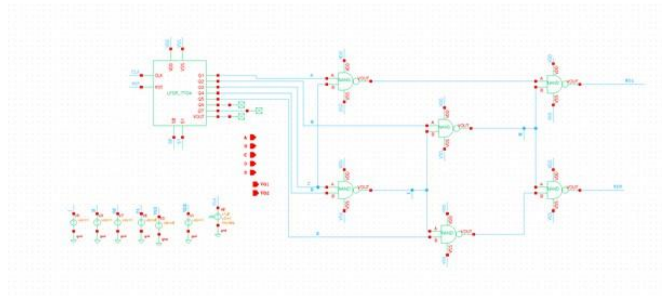

Fig. 11: Waveform for 5 input faultfree CUT

Sl No.	A	B	C	E	F	VOUT Calculated	VOUT Actual
1	0	1	1	1	1	1	1
2	0	1	1	0	0	1	1
3	1	0	1	1	0	0	0
4	0	1	0	1	1	1	1
5	0	0	1	0	1	0	0

Fig. 12: Comparison table of 5 input faultfree CUT

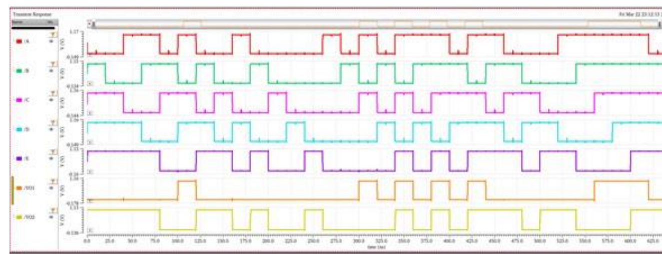

Fig. 13: Waveform for 5 input Struck at fault 1 at pos1 and 2

Sl No.	A	B	C	E	F	VOUT Calculated	VOUT Actual	VOUT Fault free
1	0	1	1	1	1	1	1	1
2	0	1	1	0	0	1	1	1
3	1	0	1	1	0	1	1	0
4	0	1	0	1	1	1	1	1
5	0	0	1	0	1	1	1	0

Fig. 14: Comparison table of 5 input faulty CUT i.e.,Struck at fault 1 at pos1 and 2

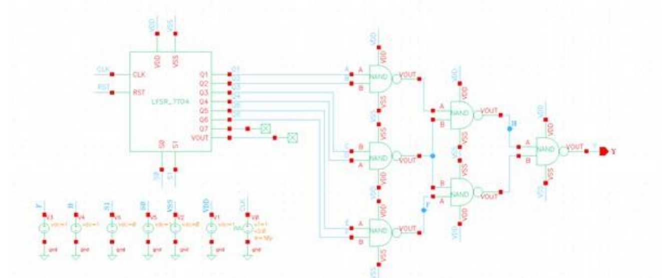

Fig. 15: LFSR with 6 input CUTS with labled position 1 and 2

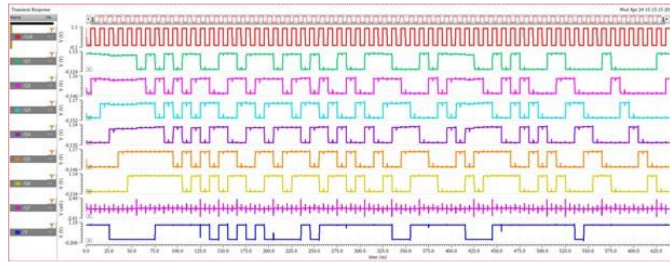

Fig. 16: Waveform for 6 input faultfree CUT

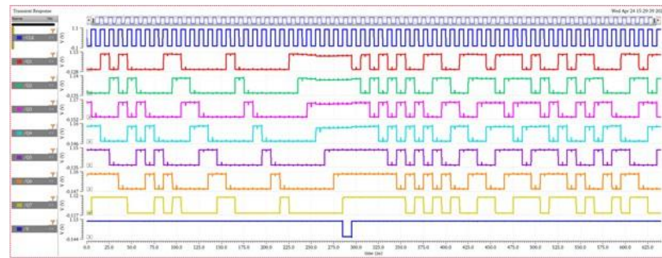

Fig. 17: Comparison table of 6 input faultfree CUT

SI No.	A	B	C	D	E	F	VOUT Calculated	VOUT Actual
1	1	1	0	0	0	0	1	1
2	1	1	1	0	0	0	1	1
3	1	1	1	1	0	0	0	0
4	1	1	1	1	1	0	1	1
5	1	1	1	1	1	1	0	0

Fig. 18: Waveform for 6 input Struck at fault 1 at pos1 and 2

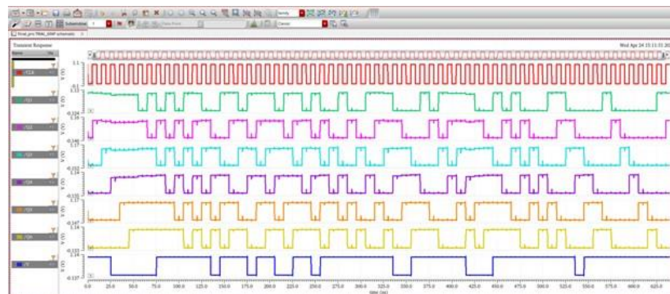

Fig. 19: Comparison table of 6 input faulty CUT i.e.,Struck at fault 1 at pos1 and 2

SI No.	A	B	C	D	E	F	VOUT Calculated	VOUT Actual	VOUT Fault free
1	1	1	0	0	0	0	1	1	1
2	1	1	1	0	0	0	1	1	1
3	1	1	1	1	0	0	0	0	0
4	1	1	1	1	1	0	0	0	1
5	1	1	1	1	1	1	0	0	0

Fig. 20: LFSR with 7 input CUT with labled position 1 and 2

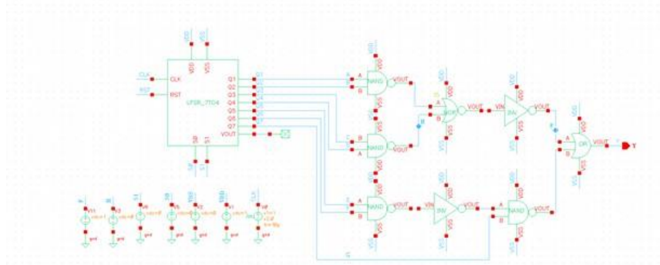

Fig. 21: Waveform for 7 input faultfree CUT

SI No.	A	B	C	D	E	F	G	VOUT Calculated	VOUT Actual
1	1	1	0	0	0	0	1	1	1
2	1	1	1	1	1	1	1	0	0
3	0	1	1	1	1	1	1	1	1
4	1	0	1	1	1	1	1	1	1
5	0	1	0	1	1	1	1	1	1

Fig. 22: Comparison table of 7 input faultfree CUT

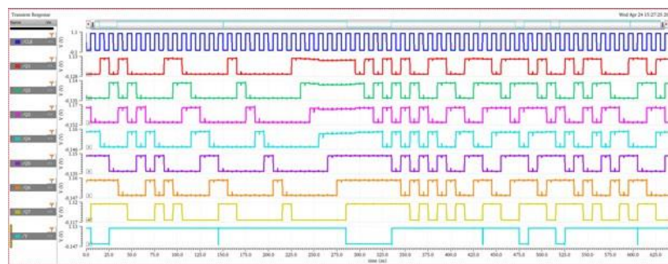

Fig. 23: Waveform for 7 input Struck at fault 0 at pos1 and 2

SI No.	A	B	C	D	E	F	G	VOUT Calculated	VOUT Actual	VOUT Fault free
1	0	0	1	1	1	1	0	1	1	1
2	0	0	0	1	1	1	1	0	0	1
3	1	0	0	0	1	1	1	0	0	1
4	0	1	0	0	0	0	1	1	1	1
5	1	0	1	0	0	0	1	1	1	1

Fig. 24: Comparison table of 7 input faulty CUT i.e.,Struck at fault 0 at pos1 and 2

6. CONCLUSION

To summarize, the use of multi-bit TPGs with dynamic LFSR selection demonstrates a robust BIST architecture ca- pable of identifying flaws and defects in integrated circuits. The comprehensive testing and fault detection procedures in place help to ensure the dependability and integrity of digital circuit designs. This emphasizes the crucial need of rigorous testing procedures in the realm of current integrated circuit design processes. The findings support the effectiveness of our technique in improving TPG fault detection capabilities, hence contributing to the improvement of IC testing technology.

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